DOI: https://doi.org/10.52756/ijerr.2023.v30.006 ***Int. J. Exp. Res. Rev.*, Vol. 30: 57-62 (2023)**

Original Article | *Peer Reviewed* | *Open Access*

International Journal of Experimental Research and Review (IJERR)

ISSN: 2455-4855 (Online)
www.iaph.in
ISSN 2455-4855

Design of low voltage high output resistance current mirror

Mallipeddi Anitha[1]*, Gonugunta Venkata Prasanna Anjaneyulu[2], Praveena Bai Desavathu[3] and Yarlagadda Mallikharjuna Rao[4]

[1,2,4]EEE Department, RVR & JC College of Engineering, Guntur 522019, Andhra Pradesh, India;
[3]ECE Department, PVP Siddhartha Institute of Technology, Vijayawada 520007, Andhra Pradesh, India

E-mail/Orcid Id:

MA, mallipeddianitha@gmail.com, https://orcid.org/0000-0002-5771-6638; *GVPA,* gvp.anjaneyulu@gmail.com, https://orcid.org/0000-0003-1120-7421; *PBD,* praveena.d@pvpsiddhartha.ac.in, https://orcid.org/0000-0002-0579-2380; *YMR,* ymallieee@gmail.com, https://orcid.org/0000-0002-3280-6530

Article History:

Received: 17th Feb., 2023
Accepted: 22nd Mar., 2023
Published: 30th Apr., 2023

Keywords:
Bandwidth, feedback, input node, output resistance, supply, voltage follower.

Abstract: A current mirror design having high output resistance operating at low supply voltage is proposed in this paper. The low voltage operation is achieved using the flipped voltage follower for current mirroring. The circuit operates at low supply with high swing with low impedance node at its output. As low impedance is one the basic requirement of a current mirror, the flipped voltage follower when used as an input shows reduced impedance. However, the observed output resistance of conventional flipped voltage follower current mirror turns to be around 700K ohm, a low value. So, for its improvement a feedback loop is used at the output of proposed current mirror. This improves the output resistance significantly without deteriorating the other performances like bandwidth to a value of 401M ohm. The proposed current mirror results in input impedance in hundreds of ohms around 330 ohm and bandwidth of 2.4GHz comparatively higher than its conventional design. The complete design is carried out using 180 nanometer-based MOS transistors and the circuit runs at 0.5 volt of dual polarity.

Introduction

Today, especially for portable devices, low power is a basic constraint to be met for long battery life. In such a scenario, the traditional circuits fail to meet the requirement. The need to redesign the circuits at lower technology which should be functionable at reduced supply is a major concern with designers. Though the scaled technology helps in reducing the power by demanding low supply but at the same time the second-order effects become prominent if the design is analog. In digital such effects do not deteriorate the performance much. In any IC, the performance is decided by the components used for its construction. If the sub-blocks used in an IC consume less power, it means the overall system performance will be better. For an analog IC, current mirror is one of the fundamental blocks which is widely used in most of the circuits. The ideal feature of a current mirror includes a large dynamic range, wide bandwidth, reduced input resistance and high output resistance. However, in nanometer technology the threshold voltage puts a challenge in circuit realization. The fact is threshold voltage does not scale in proportion to technology. To address this, low voltage design techniques is reported in literature. One is based on transistor level which is commonly referred in literature as non-conventional approach (Blalock et al., 1998; Rajput and Jamuar, 2001; Hasler and Lande, 2001; Ramirez-Angulo et al., 2004; Khateb, 2015; Della et al., 2022). Such includes bulk driven and its hybrid forms. Current mirrors based on such an approach can be found as based on FG (Sharma et al., 2006; Manhas et al., 2008; Aggarwal, 2022), based on QFG (Gupta and Sharma, 2012; Esparza-Alfaro et al., 2014; Raj et al., 2014a), and based on BDQFG (Raj et al., 2014b, 2015, 2016; Doreyatim et al., 2019). The other possible way is to make changes at circuit implementation level like one of the frequently used approaches is flipped voltage follower (Carvajal et al., 2005). This is generally cited as a low voltage cell and is useful in many analog designs. In this work, the flipped voltage follower based current

***Corresponding Author:** mallipeddianitha@gmail.com

mirror is proposed. The reason for using flipped voltage follower is its low output impedance node. Such nodes are basic key requirements of a current mirror. Recent literature based on flipped voltage follower based current mirror exploiting the low impedance node advantage can be found in (Bchir et al., 2020; Shrivastava et al., 2020; Raj, 2021; Vidhate and Suman, 2021; Kumar et al., 2021, 2022). This also helped in reducing the input compliance voltage requirement. For other parameter improvement like output resistance and bandwidth, a feedback topology (Safari and Azhari, 2013) is used in the proposed architecture. This introduces a scaling factor, square of the intrinsic gain in the output resistance due to which significant improvement is seen. The feedback does change the output resistance in mega ohms range without degrading other performance parameters when compared with conventional flipped voltage follower current mirror.

The paper is organized in a way: basics of flipped voltage follower is covered in section 2 followed by brief discussion on conventional and proposed flipped voltage follower current mirrors. This also includes small signal analysis of proposed circuit. The results are discussed in section 4 and the conclusion is drawn in section 5.

Methods

The flipped voltage follower (FVF) is a structure basically a source follower. This structure operates at low supply. The advantage with such structure compared to source follower is low impedance at its output node. Additionally, it offers a high swing. The schematic of conventional FVF is shown in figure 1.

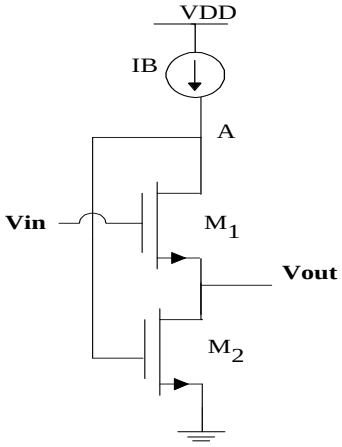

Figure 1. Flipped voltage follower

It consists of shunt feedback which results in effective output impedance as $[1/(gm_2gm_1r_{01})]$ where gm_i and r_{0i} is the trans-conductance of MOSFET and output resistance of the MOSFET. This fulfills the requirements of circuits which require low impedance nodes like current mirror.

Proposed Work

The architecture of conventional FVF current mirror is shown in figure 2.

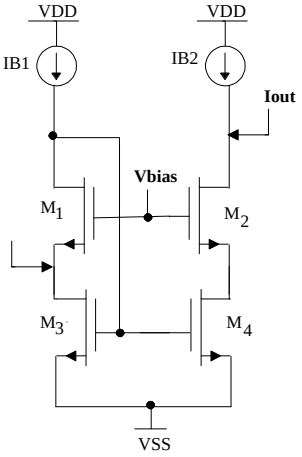

Figure 2. Conventional FVF current mirror

In the architecture, I_{in} is the input current applied to the FVF stage, which here is the drain end of M1. As drain impedance is low enough, the input resistance of realized current mirror is sufficiently low. The mathematical analysis yields the input resistance as $(1/g_{m1}g_{m3}r_{03})$ ranging in ohms and output resistance as $(g_{m4}r_{04}r_{02})$ ranging in kilo ohms for the conventional FVF current mirror.

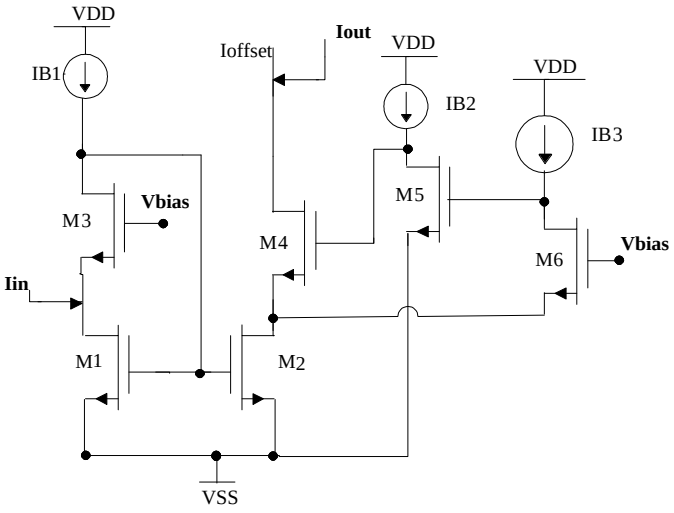

Figure 3. Proposed FVF current mirror

However, in most cases, the requirement is reduced input and sufficiently high output resistance like in mega ohms. So, to achieve such an output section is incorporated with a feedback network in the proposed current mirror. The architecture of the modified current mirror proposed is shown in figure 3. Here transistors M4, M5 and M6 along with current sources IB2 and IB3 are used to realize the network. Using this feedback network, a multiple factor of $[(g_{m5}r_{05})\ (g_{m6}r_{06})]$ is introduced in the output resistance which significantly boosted resistance level. As the feedback is locally

DOI: https://doi.org/10.52756/ijerr.2023.v30.006

generated the current mirror remains stable and such changes also do not affect the other performance parameters. The drain of M4 acts as output node.

Small signal analysis

The mathematical analysis comprises of input and output resistances of proposed FVF current mirror.

Input resistance

The model for input resistance calculation is shown in figure 4.

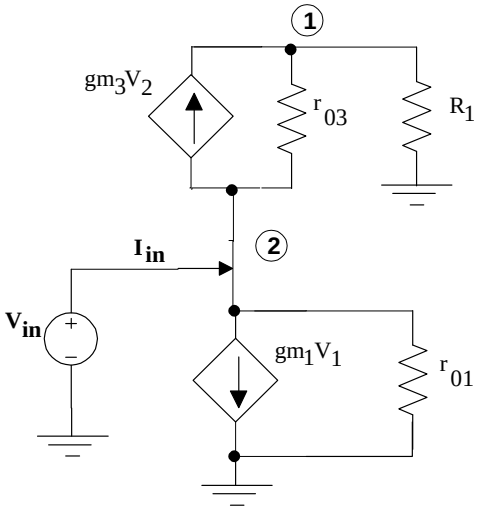

Figure 4. Input resistance calculation

At node 2

$$i_{in} - \frac{V_1}{R_1} - g_{m1}V_1 - \frac{V_2}{r_{01}} = 0 \quad \text{(1)}$$

At node 1

$$g_{m3}V_2 + \frac{V_2 - V_1}{r_{03}} - \frac{V_1}{R_1} = 0 \quad \text{(2)}$$

Solving (2)

$$V_1 = \left(\frac{g_{m3}r_{03}+1}{r_{03}}\right)(r_{03}//R_1)V_2 \quad \text{(3)}$$

Since $g_m r_0 >> 1$

$$V_1 \approx g_{m3}(r_{03}//R_1)V_2 \quad \text{(4)}$$

From (1) & (4)

$$i_{in} = \left(\frac{1}{R_1} + g_{m1}\right)V_1 + \frac{V_2}{r_{01}} \quad \text{(5)}$$

$$i_{in} = \left(\left(\frac{1}{R_1} + g_{m1}\right)g_{m3}(r_{03}//R_1) + \frac{1}{r_{01}}\right)V_2 \quad \text{(6)}$$

$$i_{in} = g_{m1}g_{m3}(r_{03}//R_1)V_{in} \quad \text{(7)}$$

$$R_{in} = \frac{V_{in}}{i_{in}} \approx \frac{1}{g_{m1}g_{m3}(r_{03}//R_1)} \quad \text{(8)}$$

For an ideal current source, $R_1 = \infty$

$$R_{in,prop.} \approx \frac{1}{(g_{m3}r_{03})g_{m1}} = R_{in,conv.} \quad \text{(9)}$$

Here since no change has been made on the input section so the resistance level remains equal to conventional design.

Output resistance

The model for output resistance calculation is shown in figure 5.

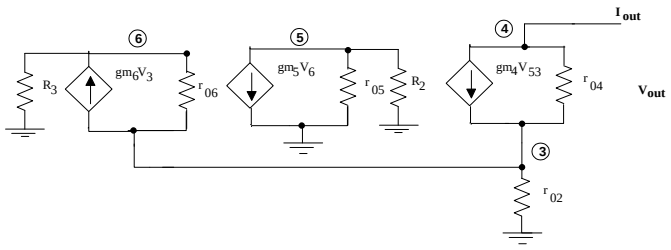

Figure 5. Output resistance calculation

At node 4

$$i_{out} = g_{m4}V_{53} + \frac{V_4 - V_3}{r_{04}} \quad \text{(10)}$$

At node 5

$$g_{m5}V_6 + \frac{V_5}{r_{05}} + \frac{V_5}{R_2} = 0 \quad \text{(11)}$$

$$V_5 = -g_{m5}(r_{05}//R_2)V_6 \quad \text{(12)}$$

At node 6

$$-g_{m6}V_3 + \frac{V_6 - V_3}{r_{06}} + \frac{V_6}{R_3} = 0 \quad \text{(13)}$$

$$V_6 = g_{m6}(r_{06}//R_3)V_3 \quad \text{(14)}$$

From (12) & (14)

$$V_5 = -g_{m5}g_{m6}(r_{05}//R_2)(r_{06}//R_3)V_3 \quad \text{(15)}$$

$$V_{53} = -g_{m5}g_{m6}(r_{05}//R_2)(r_{06}//R_3)V_3 \quad \text{(16)}$$

$$i_{out} = -g_{m4}g_{m5}g_{m6}(r_{05}//R_2)(r_{06}//R_3)r_{02}i_{out} - \frac{r_{02}i_{out}}{r_{04}} + \frac{V_4}{r_{04}} \quad \text{(17)}$$

$$R_{out} = \frac{V_4}{i_{out}} = r_{02} + r_{04} + r_{02}g_{m4}g_{m5}g_{m6}r_{04}(r_{05}//R_2)(r_{06}//R_3) \quad \text{(18)}$$

Since $g_m r_0 >> 1$

$$R_{out,prop.} \approx (g_{m4}r_{04})g_{m5}(r_{05}//R_2)g_{m6}(r_{06}//R_3)r_{02} \quad \text{(19)}$$

For an ideal current source, $R_2 = R_3 = \infty$

$$R_{out,prop.} \approx (g_{m4}r_{04})(g_{m5}r_{05})(g_{m6}r_{06})r_{02} \quad \text{(20)}$$

While for conventional FVF current mirror it is

$$R_{out,conv.} \approx (g_{m4}r_{04})r_{02} \quad \text{(21)}$$

As seen from (20) & (21), due to feedback a factor $(g_m r_0)^2$ gets multiplied to the output resistance which increases the value of resistance to mega ohm range without deteriorating the bandwidth response.

Results and Discussion

The current mirrors shown as in figure 2 and figure 3, conventional and proposed are simulated in 180 nanometer technology with the help of 0.5 volt of dual

DOI: https://doi.org/10.52756/ijerr.2023.v30.006

polarity. For simulation, the width of the transistors chosen along with other parameters assumed is shown in table 1. The length of all the MOS transistors is set to 240 nanometers.

Table 1. Width and other parameters.

MOSFET	W(nm)	Assumptions
M1, M2	25000	supply= ± 0.5V, IB1=30uA, IB2=IB3=100uA, Ioffset=5uA
M3, M4, M6	5000	
M5	240	

The simulated results match with the analysis carried out. In figure 6, the current transfer characteristics plot for conventional and proposed both is shown. The linearity does not get affected by the incorporated changes and the circuit performs its mirroring till 500 micro amperes. For the same, the percentage error in current transfer is shown in figure 7 where for the proposed FVF current mirror as expected has reduced error compared to conventional design. The reason behind is the increased output resistance. With the increase in magnitude of input current, the errors do not rise significantly.

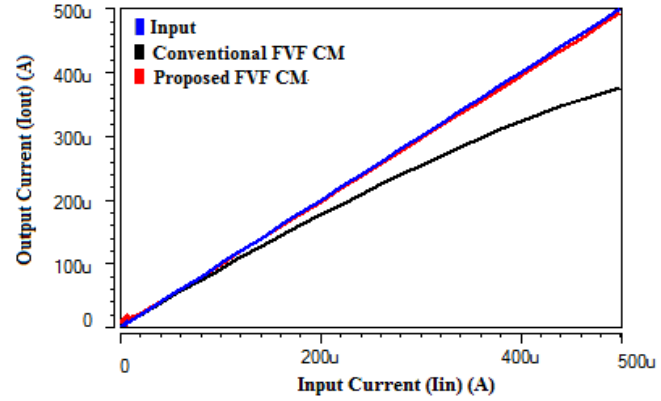

Figure 6. Current transfer characteristics of conventional and proposed FVF current mirror for input current ranging from 0 to 500uA

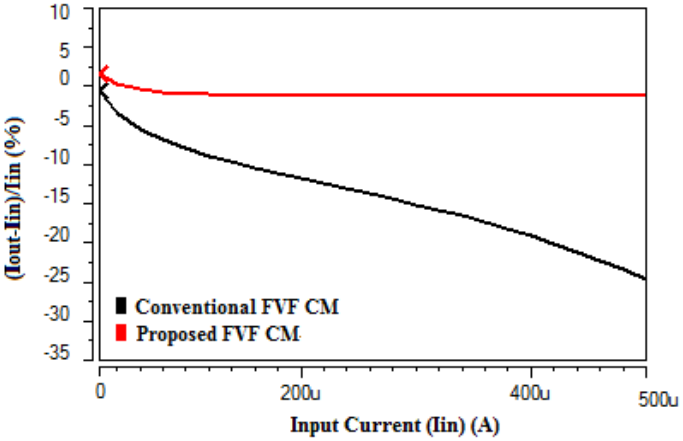

Figure 7. Percentage error in conventional and proposed FVF current mirror for input current ranging from 0 to 500uA

The output characteristic is shown in figure 8 where the degradation is seen in case on conventional FVF current mirror for higher input current. The output characteristic for proposed circuit shows minimal error even for 500 micro ampere current.

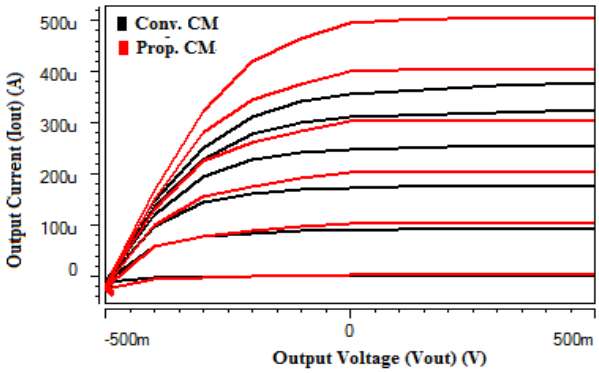

Figure 8. Output characteristics of conventional and proposed FVF current mirror for input current ranging from 0 to 500uA in steps of 100uA

The output resistance and frequency response plots are shown in figure 9 and 10 respectively. The proposed current mirror's output resistance in figure 9 as discussed gets significantly boosted due to feedback network. The value for proposed FVF current mirror is calculated to be 401M ohms whereas 700K ohms is found for conventional FVF current mirror which is far lesser than proposed. It means a 550 times better resistance is achieved.

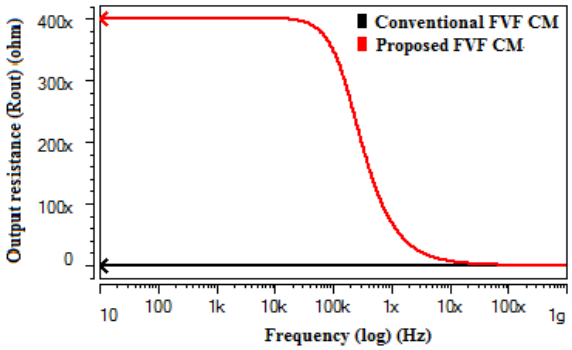

Figure 9. Output resistance of conventional and proposed FVF current mirror

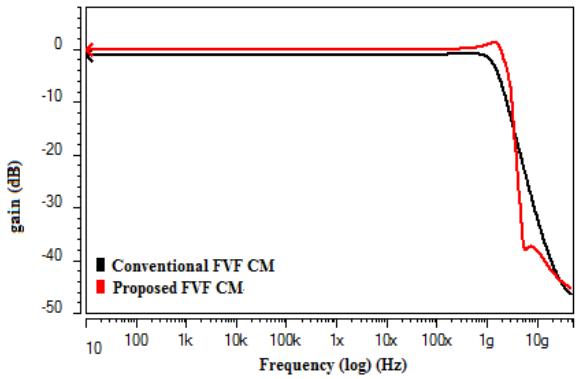

Figure 10. Frequency responses of conventional and proposed FVF current mirror

DOI: https://doi.org/10.52756/ijerr.2023.v30.006

However, in the case of bandwidth in figure 10, a slight improvement is achieved which is 2.4G Hz whereas for conventional it is 1.4G Hz. The overall results are shown in tabular form and compared with the prior work as shown in table 2.

Table 2. Comparison of performance parameters

Para-meters	Bchir et al., 2020	Shrivastava et al., 2020	Raj, 2021	Kumar et al., 2021	Kumar et al., 2022	FVF CM (Fig. 2)	Prop. FVF CM (Fig. 3)
Current range (uA)	0-200	0-150	0-500	0-500	0-200	0-500	0-500
Error (%)	0.2	4.9	-0.4	---	----	-23.5	-1.29
Input resistance (ohm)	130	12K	170	2.88K	820	330	330
Output resistance (ohm)	9.5G	---	750K	2.77M	32M	0.7M	401M
-3db frequency (HZ)	2.7G	624M	4.5G	1.93G	2.2G	1.4G	2.4G
Supply (V)	0.8	1.2	± 0.5	± 0.5	± 0.5	± 0.5	± 0.5
Technology (um)	0.18	1.18	0.18	0.18	0.18	0.18	0.18

Conclusion

The FVF based current mirror circuit with boosted output resistance is proposed in this paper. The FVF is widely used for low voltage circuit implementation & so using in current mirror helps to design low voltage current mirror architecture. In the proposed current mirror, the modification is carried out through locally generated negative feedback which does not require any compensation and so without increasing the complexity the improvement is achieved. The achieved performance and mega ohms output resistance encourages its application for high bandwidth precise VLSI system design.

Conflict of Interest

The authors declare no conflict of interest.

References

Aggarwal, B. (2022). Novel Current Mirrors Based on Folded Flipped Voltage Follower Configuration. *Wireless Personal Communications*, *123*, 645–653. https://doi.org/10.1007/s11277-021-09150-3

Blalock, B.J., Allen, P.E., & Rincon-Mora, G. (1998). Designing 1-V op amps using standard digital CMOS technology. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, *45*(7), 769-780. https://doi.org/10.1109/82.700924

Bchir, M., Aloui, I., & Hassen, N. (2020). A bulk-driven quasi-floating gate FVF current mirror for low voltage, low power applications. *Integration*, *74*, 45-54. https://doi.org/10.1016/j.vlsi.2020.04.002

Carvajal, R. G., Ramirez-Angulo, J., Lopez-Martin, A. J., Torralba, A., Galan, J. A. G., Carlosena, A., & Chavero, F. M. (2005). The flipped voltage follower: a useful cell for low-voltage low-power circuit design. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *52*, 1276-1291. https://doi.org/10.1109/TCSI.2005.851387

Della, S.R., Centurelli, F., Scotti, G., Tommasino, P., & Trifiletti, A. (2022). A Differential-to-Single-Ended Converter Based on Enhanced Body-Driven Current Mirrors Targeting Ultra-Low-Voltage OTAs. *Electronics*, *11*, 3838. https://doi.org/10.3390/electronics11233838

Doreyatim, M. S., Akbari, M., & Nazari, M. (2019). A low-voltage gain boosting-based current mirror with high input/output dynamic range. *Microelectronics Journal*, *90*, 88-95. https://doi.org/10.1016/j.mejo.2019.05.022

Esparza-Alfaro, F., Lopez-Martin, A.J., Carvajal, R.G., & Ramirez-Angulo, J. (2014). Highly linear micropower class AB current mirrors using Quasi-Floating Gate transistors. *Microelectronics Journal*, *45*(10), 1261-1267. https://doi.org/10.1016/j.mejo.2014.02.006

Gupta, R., & Sharma, S. (2012). Quasi-floating gate MOSFET based low voltage current mirror.

Microelectronics Journal, *43*(7), 439-443. https://doi.org/10.1016/j.mejo.2012.04.006

Hasler, P., & Lande, T.S. (2001). Overview of floating-gate devices, circuits, and systems. *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, *48*(1), 1-3. https://doi.org/10.1109/TCSII.2001.913180

Khateb, F. (2015). The experimental results of the bulk-driven quasi-floating-gate MOS transistor. *AEU-International Journal of Electronics and Communications*, *69*(1), 462-466. https://doi.org/10.1016/j.aeue.2014.10.016

Kumar, P. A., Tamil, S., & Raj, N. (2021). Design of Low Voltage Quasi-floating Self Cascode Current Mirror. *U. Porto Journal of Engineering*, *7*(4), 33-45. https://doi.org/10.24840/2183-6493_007.004_0003

Kumar, P.A., Tamil, S., & Raj, N. (2022). Design of Sub-volt High Impedance Wide Bandwidth Current Mirror for High Performance Analog Circuit. *In: Advances in Intelligent Systems and Computing*, *2022*, 1413. https://doi.org/10.1007/978-981-16-7088-6_65

Manhas, P.S., Sharma, S., Pal, K., Mangotra, L.K., & Jamwal, K.K.S. (2008). High performance FGMOS-based low voltage current mirror. *Indian Journal of Pure and Applied Physics*, *46*(5), 355-358.

Rajput, S.S., & Jamuar, S.S. (2001). Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications. *IEE Proceedings-Circuits, Devices and Systems*, *148*(5), 273-278. https://doi.org/10.1049/ip-cds:20010441

Ramirez-Angulo, J., Lopez-Martin, A.J., Gonzalez-Carvajal, R., & Munoz, C.F. (2004). Very low voltage analog signal processing based on quasi floating gate transistors. *IEEE Journal of Solid State Circuits*, *39*(3), 434-442. https://doi.org/10.1109/JSSC.2003.822782

Raj, N., Singh, A.K., & Gupta, A. K. (2014a). Low power high output impedance high bandwidth QFGMOS current mirror. *Microelectronics Journal*, *45*(8), 1132-1142. https://doi.org/10.1016/j.mejo.2014.05.005

Raj, N., Singh, A.K., & Gupta, A. K. (2014b). Low-voltage bulk-driven self-biased cascode current mirror with bandwidth enhancement. *Electronics Letters*, *50*(1), 23-25. https://doi.org/10.1049/el.2013.3600

Raj, N., Singh, A.K., & Gupta, A. K. (2015). Low voltage high output impedance bulk-driven quasi-floating gate self-biased high-swing cascode current mirror. *Circuit System and Signal Processing*, *35*(8), 2683-2703. https://doi.org/10.1007/s00034-015-0184-4

Raj, N., Singh, A.K., & Gupta, A. K. (2016). Low voltage high performance bulk-driven quasi-floating gate self-biased cascode current mirror. *Microelectronics Journal*, *52*(1), 124-133. https://doi.org/10.1016/j.mejo.2016.04.001

Raj, N. (2021). Low Voltage FVF Current Mirror with High Bandwidth and Low Input Impedance. *Iranian Journal of Electrical and Electronic Engineering*, *17*, 1-7. https://doi.org/10.22068/IJEEE.17.3.1972

Sharma, S., Rajput, S.S., Mangotra, L.K., & Jamuar, S.S. (2006). FGMOS current mirror: behaviour and bandwidth enhancement. *Analog Integrated Circuits and Signal Processing*: *46*(3), 281-286. https://doi.org/10.1007/s10470-006-1625-6

Safari, L., & Azhari, S. J. (2013). A novel wide band super transistor-based voltage feedback current amplifier. *International Journal of Electronics and Communication*, *67*, 624-631. https://doi.org/10.1016/j.aeue.2013.01.005

Shrivastava, A., Pandey, R., & Jindal, C. (2020). Low-Voltage Flipped Voltage Follower Cell Based Current Mirrors for High Frequency Applications. *Wireless Personal Communication*, *111*, 143-161. https://doi.org/10.1007/s11277-019-06849-2

Vidhate, A.D. & Suman, S. (2021). Low Power High Performance Current Mirror – A Review. *Journal of Physics: Conference Series*, *1804*, 012161. https://doi.org/10.1088/1742-6596/1804/1/012161

How to cite this Article:

Mallipeddi Anitha, Gonugunta Venkata Prasanna Anjaneyulu, Praveena Bai Desavathu and Yarlagadda Mallikharjuna Rao (2023). Design of Low Voltage High Output Resistance Current Mirror. *International Journal of Experimental Research and Review*, *30*, 57-62.

DOI : https://doi.org/10.52756/ijerr.2023.v30.006