DOI: https://doi.org/10.52756/ijerr.2023.v36.031 *Int. J. Exp. Res. Rev.*, Vol. 36: 347-358 (2023)

Original Article | *Peer Reviewed* | *Open Access*

International Journal of Experimental Research and Review (IJERR)
© Copyright by International Academic Publishing House (IAPH)
ISSN: 2455-4855 (Online)
www.iaph.in
ISSN 2455-4855

Single Phase Novel H-Type Multilevel Inverter Topology with Optimal Reduction of Power Electronic Devices

Samrat Paul[1], Sourav Debnath[1*], Dipak Kumar Mandal[2] and Bidyut Mahato[3]

[1]Department of Electrical and Electronics Engineering, Swami Vivekananda Institute of Science and Technology, Kolkata-700145, West Bengal, India; [2]Department of Applied Physics, Rashbehari Siksha Prangan, University of Calcutta, Kolkata-700009, India; [3]Department of Electrical Engineering, IIT(ISM), Dhanbad, Jharkhand-826004, India

E-mail/Orcid Id:

SP, spaulrat@gmail.com ; *SD,* dr.souravdebnath@gmail.com, https://orcid.org/0000-0001-7583-0381;
DKM, dkmaphy@caluniv.ac.in; *BM,* bidyut1990@gmail.com

Article History:

Received: 13th Aug., 2023
Accepted: 17th Dec., 2023
Published: 30th Dec., 2023

Keywords:
Generalized structure, H-bridge inverter, Multilevel inverter (MLI), Nearest level control (NLC)

How to cite this Article:
Samrat Paul, Sourav Debnath, Dipak Kumar Mandal and Bidyut Mahato (2023). Single Phase Novel H-Type Multilevel Inverter Topology with Optimal Reduction of Power Electronic Devices. *International Journal of Experimental Research and Review*, *36*, 347-358.
DOI:
https://doi.org/10.52756/ijerr.2023.v36.031

Abstract: The research aims to develop a novel H-Type multilevel inverter capable of generating seventeen levels of asymmetric voltage ratios using only nine power semiconductor switches. The flexibility of this topology is that it can be extended to any desired output levels according to various algorithms suggested in this paper. Simulations are conducted using the MATLAB platform to validate the viability of the proposed topology. The results obtained from these simulations convincingly demonstrate the effectiveness of the designed inverter. Specifically, utilizing the first algorithm, voltage levels of 17, 25, 33 and 41 are generated, and various performance parameters are thoroughly examined to establish the efficacy of the topology. This research not only focuses on the development of a novel H-Type multilevel inverter capable of producing seventeen levels of asymmetric voltage ratios with a minimalistic approach of nine power semiconductor switches but also provides a pathway for extension through suggested algorithms. The validation process through MATLAB simulations and the thorough examination of performance parameters underscores the robustness and efficiency of the proposed topology.

Introduction

Over the last few decades, traditional 2-level inverters have been extensively employed in DC-AC conversion technology due to advancements in power electronic converters (Rashid, 2004). However, they suffer from various drawbacks, such as inadequate rejection of undesired harmonics in the output voltage and current, leading to excessive power dissipation and increased switch loading. To address these limitations, the multilevel inverter (MLI) was introduced in 1981 and has since gained significant importance (Franquelo et al., 2008; Rodríguez et al., 2002). MLIs outperform traditional inverter topologies in terms of their capability to generate high voltages, high efficiency, and low voltage stress into power switches, reduced harmonic currents, and minimal electromagnetic interference (EMI) (Rodríguez et al., 2007; Tolbert et al., 1999; Abu-rub et al., 2010). MLIs find crucial applications in various domains, such as FACTs, renewable and nonconventional energy systems (Mukherjee et al., 2017; Kumar and Reddy, 2023), electric drives (Carpita et al., 2008), and active filters (Jha et al., 2016). Broadly, there are three well-known classical MLIs: Neutral-Point Clamped (NPC) (Rodriguez et al., 2010), Flying Capacitor (FC-MLI) (Malekjamshidi et al., 2014), and Cascaded H-Bridge (CHB) (Ahrabi et al., 2015). H-bridge arrangements can be additionally categorized into two types i.e., symmetrical cascaded H-bridge multilevel inverters (CHB-MLI), which are

***Corresponding Author:** dr.souravdebnath@gmail.com

This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License.

characterized by DC sources with identical magnitudes, and asymmetrical cascaded H-bridge multilevel inverters (CHB-MLIs) which is distinguished by DC sources with varying magnitudes (Ahrabi et al., 2015). CHB-MLIs are commonly employed in motor drive applications (Mahato et al., 2017; Mahato et al., 2018). However, increasing the voltage level in these systems necessitates adding more power switches and corresponding gate driver circuits, resulting in a more complex and expensive circuit. Hence, reducing the number of power switches while improving efficiency, cost-effectiveness, and system performance has emerged as a major a formidable obstacle in the realm of power electronic devices.

This paper introduces a novel approach that distinguishes itself from the previously mentioned references by proposing a 17-level multilevel inverter that aims to reduce the number of necessary power switches further. The suggested arrangement is crafted with a designated count of power switches and integrates uneven magnitudes for the DC sources. A 17-level asymmetry value for the DC sources is modelled and tested using the MATLAB environment. Furthermore, a contrast is established between the newly suggested MLI configuration and several contemporary topologies (Arun et al., 2018; Samadaei et al., 2018; Gautam et al., 2018; Ajami et al., 2014; Mahato et al., 2019; Agrawal et al., 2017; Dahidah et al., 2015; Samadaei et al., 2019; Nanda et al., 2017; Alishah et al., 2017; Paul at al., 2022).

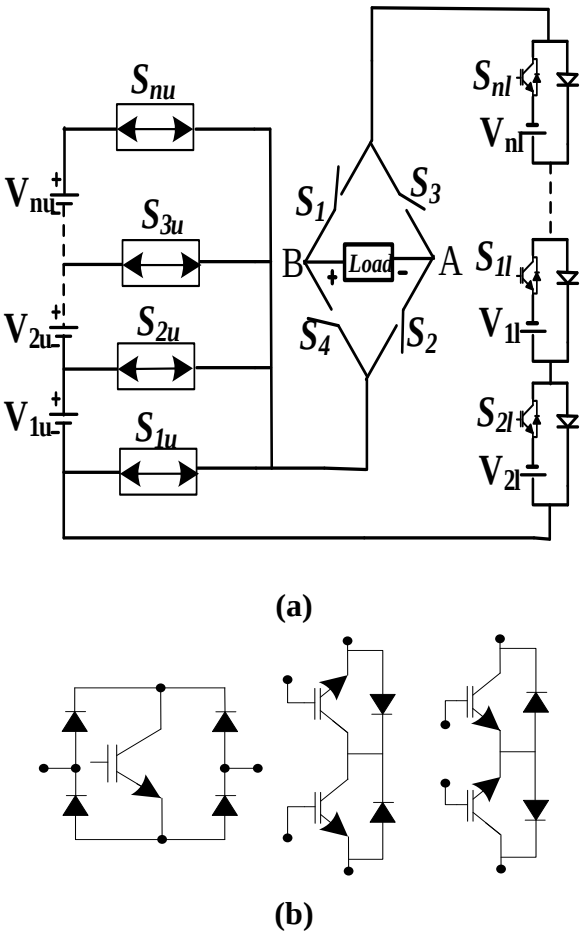


Figure 1. (a) Proposed MLI (b) Bi-directional switches

Proposed Topology (H-Type)

The suggested universal topology is illustrated in Figure 1(a); it is structured into two distinct parts: the upper part comprises bidirectional switches, while the lower part consists of unidirectional switches.

A bidirectional switch consists of IGBT and four anti-parallel diodes. Various existing configurations of bidirectional switches are detailed (Agrawal et al., 2017), as illustrated in Figure 1(b), where an IGBT switch featuring a common emitter, common collector, and four number of anti-parallel diodes is presented. The design of a bidirectional switch based on a common-collector configuration aims to reduce the voltage drop in the on-state, albeit necessitating two IGBTs and two gate drive circuits (Agrawal et al., 2017).

In a similar manner, the configuration of the common-emitter-base bidirectional switch aims to minimize the voltage drop in the on-state, but it necessitates two IGBTs and one gate drive (Agrawal et al., 2017). On the other hand, the third bidirectional switch comprises four diode IGBTs, resulting in greater conduction losses when contrasted with the aforementioned switch. While aiming for elevated voltage levels, a larger number of IGBTs, snubber circuits, common-collectors and common-emitter bidirectional switches are required. As a result, this leads to an increase in the total cost of the inverter. It is evident that a significant number of IGBTs and bidirectional switches, along with snubber circuits for common collectors and common emitters, are necessary at higher voltage levels, thereby increasing the expenses involved. In spite of the elevated conduction losses linked with bidirectional switches in the topology, the proposed configuration opts for the third type of bidirectional switch for the aforementioned reasons. For achieving N_l voltage levels, the upper part of the proposed topology requires S(n+1)u bidirectional switches, while the lower part necessitates S_{nl} unidirectional switches. Negative voltage generation is accomplished using four unidirectional power switches, namely S_1, S_2, S_3, and S_4. Depending on the magnitude and number of DC sources, various algorithms are proposed and described in Table 1. Algorithm one utilizes DC sources with magnitudes of $3V_{dc}$ and V_{dc} at the top and bottom, respectively. It has been observed that eleven power switches produce

DOI: https://doi.org/10.52756/ijerr.2023.v36.031

Table 1. Various Algorithms for the proposed multilevel inverter

Different cases	Different Input Voltage Ratio of DC sources for Proposed Multilevel Inverter		
	First algorithm (A_1)	Second algorithm (A_2)	Third algorithm (A_3)
N_{sw}=9	$V_{1u}=V_{2u}=3V_{dc}$ $V_{1l}=V_{2l}=V_{dc}$	NA	NA
N_{sw}=11	$V_{1u}=V_{2u}=V_{3u}=3V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=V_{dc}$	$V_{1u}=V_{2u}=V_{3u}=4V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=V_{dc}$	NA
N_{sw}=13	$V_{1u}=V_{2u}=V_{3u}=V_{4u}=3V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=V_{4l}=V_{dc}$	$V_{1u}=V_{2u}=V_{3u}=V_{4u}=4V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=V_{4l}=V_{dc}$	$V_{1u}=V_{2u}=V_{3u}=V_{4u}=5V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=V_{4l}=V_{dc}$
N_{sw}=15	$V_{1u}=V_{2u}=V_{3u}=V_{4u}=V_{5u}=3V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=V_{4l}=V_{5l}=V_{dc}$	$V_{1u}=V_{2u}=V_{3u}=V_{4u}=V_{5u}=4V_{dc}$ $V_{1l}=V_{2l}=V_{3u}=V_{4l}=V_{5l}=V_{dc}$	$V_{1u}=V_{2u}=V_{3u}=V_{4u}=V_{5u}=5V_{dc}$ $V_{1l}=V_{2l}=V_{3u}=V_{4l}=V_{5l}=V_{dc}$
N_{sw}	$V_{1u}=V_{2u}=V_{3u}=.....=V_{nu}=3V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=.....=V_{nl}=V_{dc}$	$V_{1u}=V_{2u}=V_{3u}=.....=V_{nu}=4V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=.....=V_{nl}=V_{dc}$	$V_{1u}=V_{2u}=V_{3u}=.....=V_{nu}=5V_{dc}$ $V_{1l}=V_{2l}=V_{3l}=.....=V_{nl}=V_{dc}$

twenty-five voltage levels according to algorithm one, while algorithm two yields thirty-one voltage levels with the same eleven power switches. Similarly, algorithm one, algorithm two, and algorithm three generate thirty-three, forty-one, and forty-nine voltage levels, respectively, using thirteen power switches. Table 1 provides a comprehensive overview of the number of voltage levels produced by a given number of switches according to algorithm one. Algorithm one demonstrates higher overall tolerance and relatively superior voltage performance compared to the other proposed algorithms. Therefore, this article primarily focuses on the various cases pertaining to algorithm one.

Modes of operation

The low-frequency modulation based NLC technique has been chosen to validate the proposed topology in the MATLAB environment. This technique is selected among other control strategies for multilevel inverters, such as selective harmonic elimination, phase-shifted modulation, sine-based carrier PWM, and the nearest level modulation technique. The low-frequency modulation-based NLC

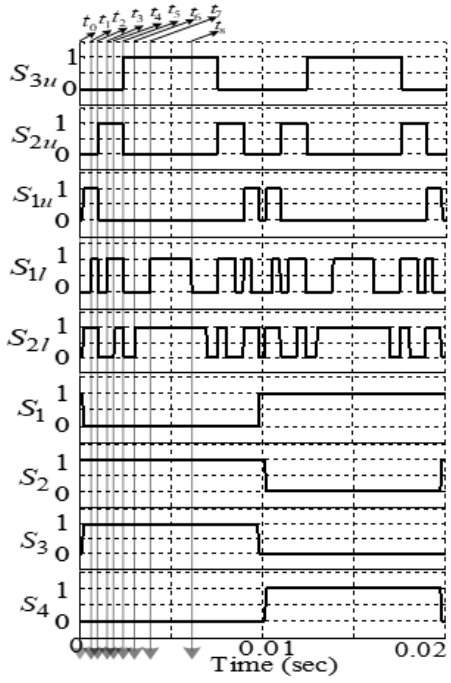


Figure 2. Pulse generated in respective power switches for 17 level inverters obtained by MATLAB/Simulink

Table 2. Comparing various performance parameters of the proposed topology with those from existing literature

Reduced components MLI	Components count				Number of output Voltage levels
	Total power switches (N_{ps})		Capacitors / DC Sources	Clamping diodes	
	Bi-directional switches	Unidirectional switches			
Arun et al., 2018	0	N_{ps}	(N_{ps}- 6)	(N_{ps}- 6)	($2N_{ps}$ - 11)
Samadaei et al., 2018	$N_{ps}/3$	$2N_{ps}/3$	$4N_{ps}/3$	0	($16N_{ps}$+9)/9
Gautam et al., 2018	$N_{ps}/7$	$6N_{ps}/7$	$3N_{ps}/7$	0	($8N_{ps}/7$)+1
Gautam et al., 2016	(N_{ps}- 6)	6	(N_{ps}- 3)	0	($4N_{ps}$ - 19)
Ajami et al., 2014	0	N_{ps}	(N_{ps}-4)/2	0	($2N_{ps}$ -7)
Mahato et al., 2019	(N_{ps}-2)	2	(N_{ps}-4)	0	($2N_{ps}$ -7)
Samadaei et al., 2016	$N_{ps}/4$	$3N_{ps}/4$	$N_{ps}/2$	0	($3N_{ps}$+2)/2
Alishah et al., 2017	(N_{ps}-6)	6	(N_{ps}-4)	0	[(N_{ps}) (N_{ps}-4)/2]+1
Alishah et al., 2016	(N_{ps}-8)	8	(N_{ps}-6)	0	[(N_{ps}-2) (N_{ps}-6)/2]+1
Proposed topology (A1)	(N_{ps}-3)/2	(N_{ps}+3)/2	(N_{ps}-5)	(N_{ps}-5)/2	($4N_{ps}$ -19)

technique is chosen because of its simplicity and ease of control. Although SHE amplifies lower-order harmonics, the substantial offline calculation of switching angles for various modulation indices can be burdensome. Sinusoidal Pulse Width Modulation (PWM) utilizes a high-frequency carrier signal to improve the Total Harmonic Distortion (THD) characteristics and reduce low-order harmonics in the recommended inverter. Furthermore, several configurations of triangular pulses, such as Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternate Phase Opposition Disposition (APOD), have been examined (Mahato et al., 2018).

NLC (Nearest Level Control) technology makes it feasible to bring the elevated voltage reference closer to the nearest attainable voltage level. This proximity aids in the synthesis of numerous voltage levels while minimizing switching losses. The NLC technique (Raushan et al., 2018) is utilized to generate the reference signal, switching signal, and their corresponding gating pulse.

DOI: https://doi.org/10.52756/ijerr.2023.v36.031

Table 3. Comparing the proposed multi-level inverter with alternative topologies

References	Year of publication	Type of configuration		Type of PWM	Requirement of H-bridge
		Symmetrical	Asymmetrical		
Arun et al., 2018	2018	Yes	Yes	Multicarrier PD-PWM	No
Samadaei et al., 2018	2018	Yes	Yes	Fundamental Switching Frequency	No
Gautam et al., 2018	2018	Yes	Yes	Multicarrier PWM	No
Gautam et al., 2016	2016	Yes	Yes	Multicarrier PWM	No
Ajami et al., 2014	2014	Yes	Yes	Multicarrier PWM	Yes
Mahato et al., 2019	2019	Yes	Yes	Multicarrier PWM	No
Proposed topology (A_1)	2023	Yes	Yes	Multicarrier PWM	Yes

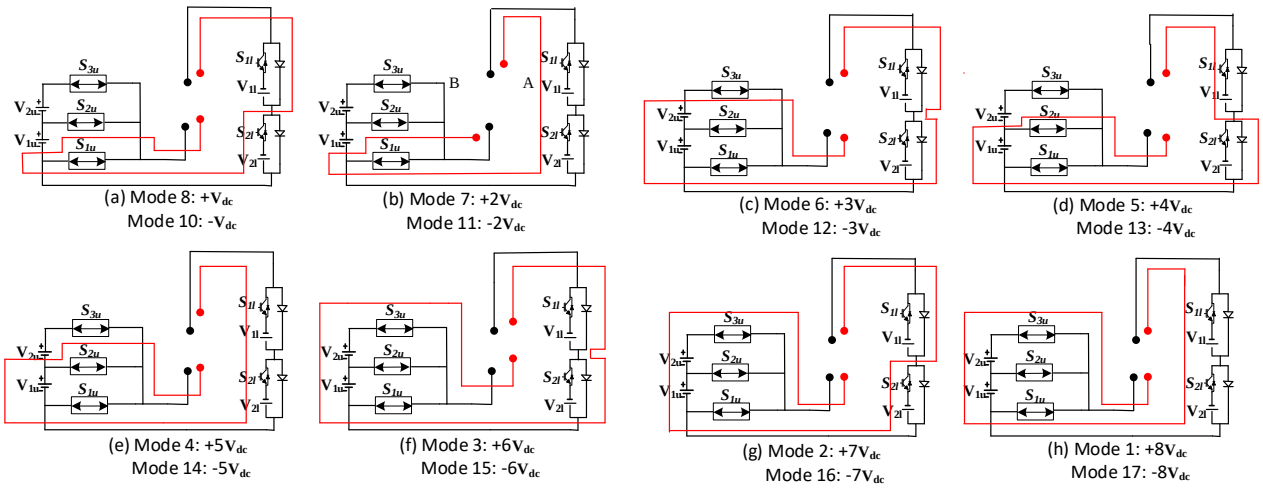


Figure 3. Modes of operation of 17 level inverter showing voltage generation paths

Figure 3 provides a comprehensive illustration of the various voltage generation modes. The dark lines in figure 3 depict the voltage generation paths of the proposed topology specifically designed for a 17-level inverter. The switching patterns for each switch are obtained from the simulations presented in figures 2(a)

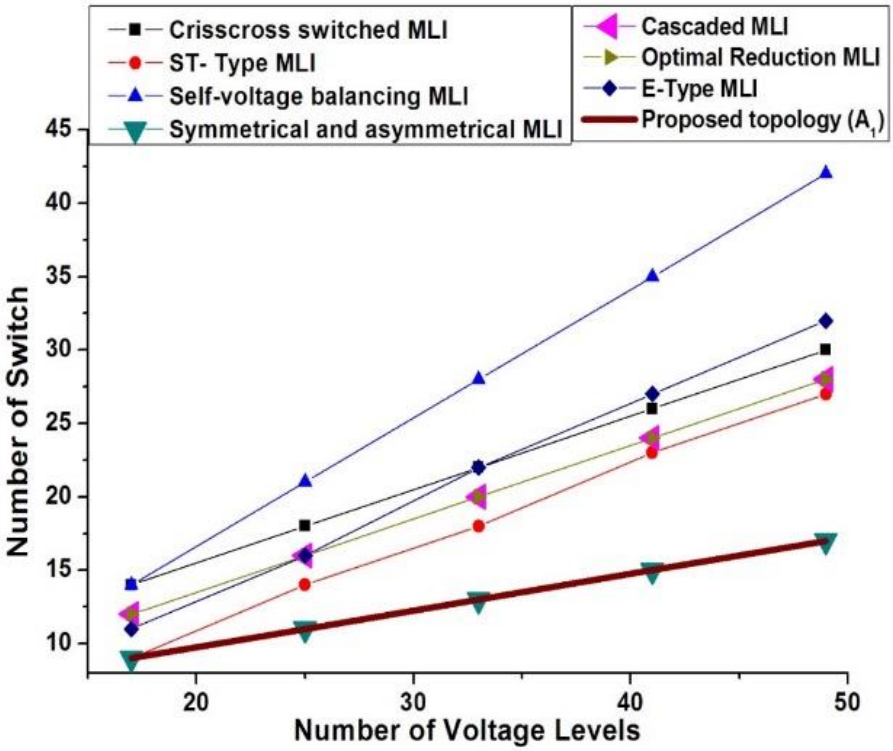
DOI: https://doi.org/10.52756/ijerr.2023.v36.031

and 2(b) correspondingly. A full bridge circuit is utilized to generate both negative and positive polarities. Switches S_3 and S_4 are responsible for generating positive voltage levels, while switches S_1 and S_2 are employed to produce negative voltage levels. Figure 3 visually illustrates the voltage levels produced by the upper and lower sections of the proposed topology.

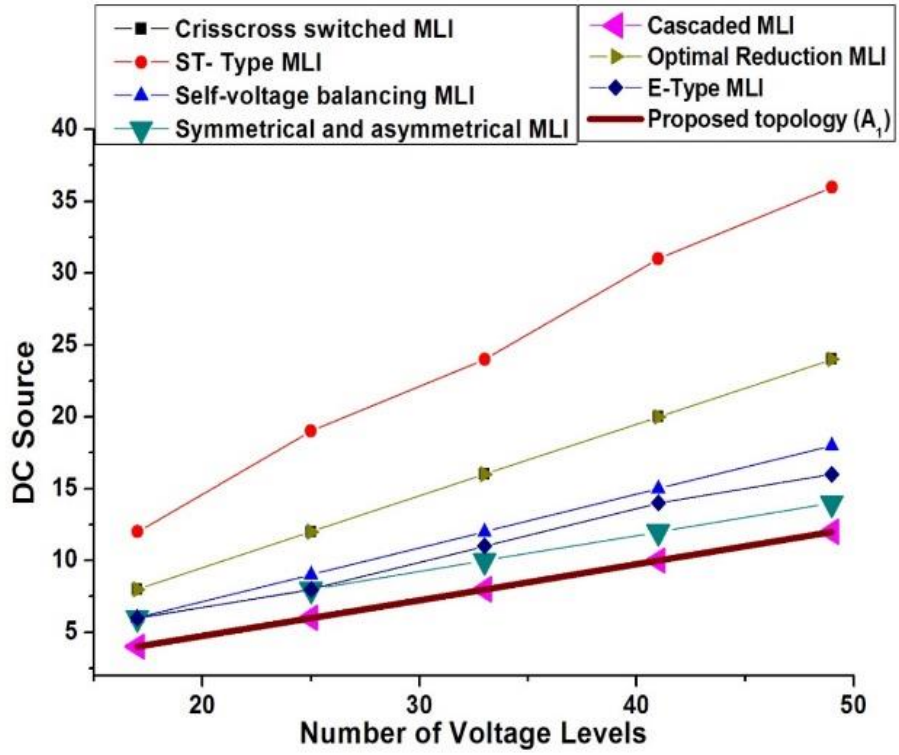
Comparison with existing MLIs

Extensive research has been conducted on the existing literature regarding reduced switch topologies (Arun et al., 2018; Samadaei et al., 2018; Gautam et al., 2016 and 2018; Ajami et al., 2014; Mahato et al., 2019; Agrawal et al., 2017; Dahidah et al., 2015; Samadaei et al., 2019; Nanda et al., 2017; Alishah et al., 2017; Paul at al., 2022), focusing on several important parameters. These parameters include the required quantities of total power switches (N_{ps}), DC sources (N_{DC}), unidirectional switches (N_{us}), clamping diodes (N_{cl}), bidirectional switches (N_{bs}), and output voltage levels (N_{vl}).

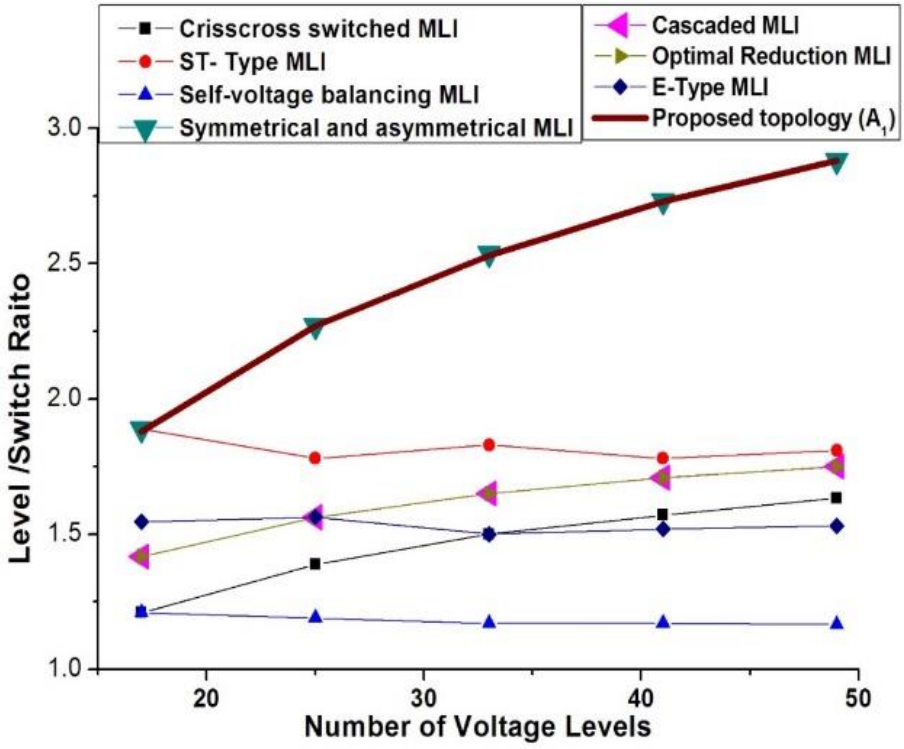
Table 2 provides generalized equations for all the parameters described previously in order to demonstrate the effective behaviour of the suggested inverter architecture. These expressions are formulated in terms of the total number of switches (N_{ps}). Furthermore, corresponding generalized expressions are computed and summarized in Table 2 to simplify the calculation of these parameters. A comparative analysis is also conducted, focusing on the total number of switches, number of DC power supplies, and level per switch ratio. Additionally, Table 3 includes additional features and disadvantages of these multilevel inverter configurations, aiming to demonstrate the effectiveness of the proposed topology. A thorough analysis is conducted, comparing the MLI topologies (Samadaei et al., 2018; Gautam et al., 2016; Gautam et al., 2018; Mahato et al., 2019), which employ both unidirectional and bidirectional switches. The MLI structures discussed in (Arun et al., 2018; Ajami et al., 2014) use only switches that can conduct electricity in one way. However, the expense and complexity of achieving higher voltage levels rise due to the greater number of power switches and the driving circuits needed. Table 3 provides a comprehensive analysis of the construction of the multilevel inverter.



(a)



(b)



(c)

Figure 4. Performance parameters of the proposed topology based on A1 algorithm (a) Number of switch (N_{ps}) versus Number of voltage levels (b) Number of DC sources versus Number of voltage levels (c) Level/ Switch ratio versus Number of voltage levels.

A comparative analysis has been conducted of the recent studied literature (Arun et al., 2018; Samadaei et al., 2018; Gautam et al., 2018; Ajami et al., 2014; Mahato et al., 2019; Agrawal et al., 2017; Dahidah et al., 2015; Samadaei et al., 2019; Nanda et al., 2017; Alishah et al., 2017; Paul at al., 2022) and the proposed topologies based on the A1 algorithm. Figure 4 presents graphical representations of this analysis. Figure 4(a) depicts the

DOI: https://doi.org/10.52756/ijerr.2023.v36.031

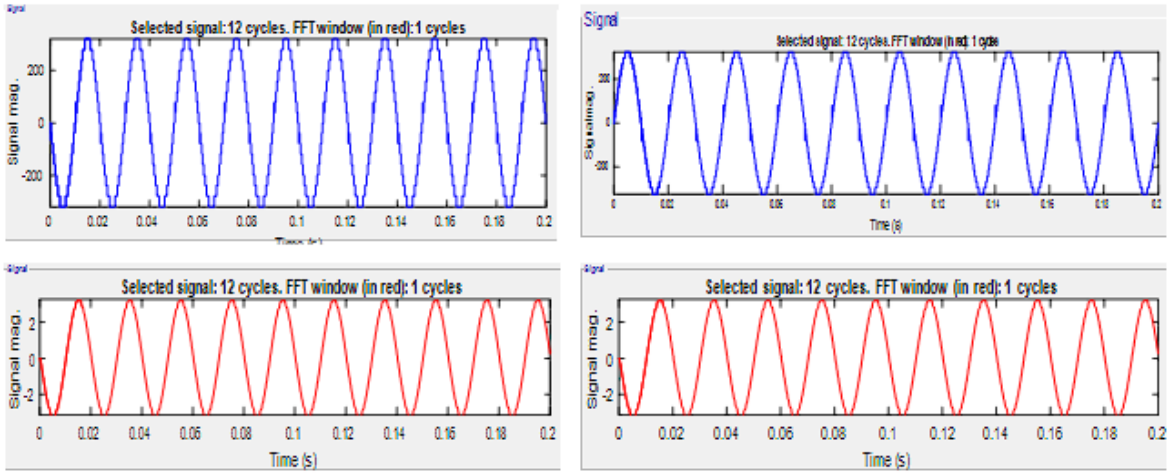
correlation between the quantity of switches (Nps) and the quantity of voltage levels. Figure 4(b) illustrates the relationship between the quantity of DC sources and the number of voltage levels. Finally, Figure 4(c) illustrates the graph representing the output level per switch. The comparative analysis revealed that the proposed topology, which utilizes the A1 algorithm, produces a higher quantity of voltage levels while using the same number of power switches compared to the topologies of multilevel inverters (Arun et al., 2018; Samadaei et al., 2018; Gautam et al., 2018; Ajami et al., 2014; Mahato et al., 2019; Agrawal et al., 2017), as shown in Figure 4(a).

The suggested topology based on the A1 algorithm outperforms alternative topologies in terms of the number of DC sources required to obtain the same number of voltage levels, as shown in Figure 4(b). In addition, this study determines the ratio of switching levels for the proposed multilevel inverter and the already used reduced-switch multilevel inverters. This ratio indicates the amount of power devices needed to provide the necessary output voltage levels. Figure 4(c) presents the level to switch ratio for both the proposed and recent reduced-switch multilevel inverters, considering a total of twenty-one power devices. The proposed multilevel inverter configuration requires significantly fewer switches (Nps) than the other reduced-switch multilevel inverters.

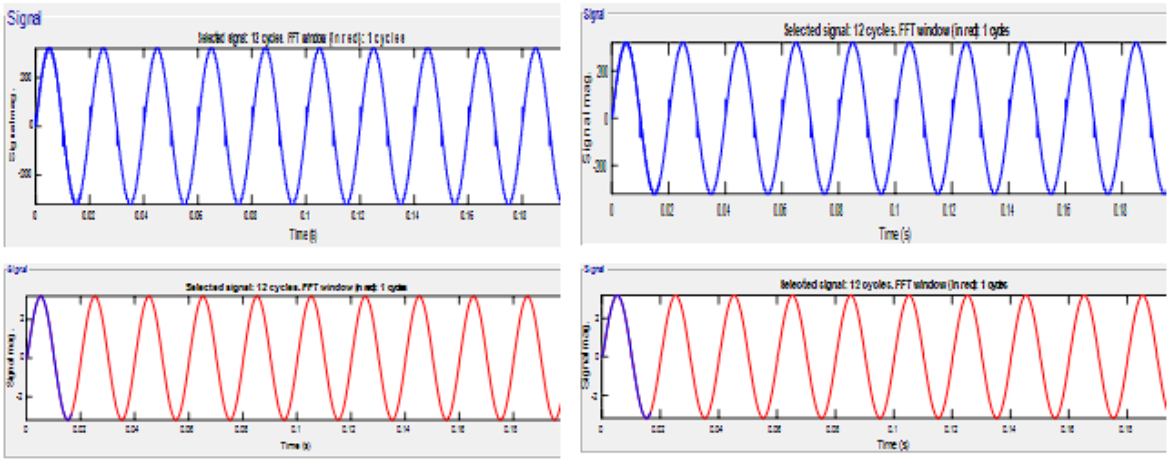
Simulation Verification

This study focuses on conducting simulation validation of the proposed inverter, specifically based on algorithm-1 (A1).

Table 1 presents a comprehensive overview of numerous scenarios, each dependent on a distinct number of power switches. Utilizing the A1 algorithm, the suggested design demonstrates the capacity to produce seventeen distinct voltage levels by employing nine power switches and four DC sources. In addition, it can attain 25 voltage levels using 11 power switches and 6 DC sources, 33 voltage levels using 13 power switches and 8 DC sources, and 41 voltage levels using 15 power



(a)V_{pk}=320V (b)V_{pk}=324V



(c)V_{pk}=320V (d)V_{pk}=320V

Figure 5. Various simulation results of output voltage and output current across RL load at R=100Ω, L=25mH for (a) 17-level inverter, (b) 25-level inverter, (c) 33-level inverter, (d) 41-level inverter.

DOI: https://doi.org/10.52756/ijerr.2023.v36.031

switches and 10 DC sources. To thoroughly assess the performance of each circuit, all the aforementioned configurations are meticulously modelled and simulated in the MATLAB/Simulink environment.

Furthermore, the magnitudes of the DC sources corresponding to the different cases of the proposed topology, based on the A1 algorithm, are detailed. "DC sources are considered as $V_{1u}=V_{2u}=3V_{dc}=120V$; $V_{1l}=V_{2l}=V_{dc}=40V$ for the seventeen level inverter with a peak magnitude of 320V, $V_{1u}=V_{2u}=V_{3u}=3V_{dc}=81V$; $V_{1l}=V_{2l}=V_{3l}=V_{dc}=27V$ for the twenty-five level inverter with a peak magnitude of 324V, $V_{1u}=V_{2u}=V_{3u}=V_{4u}=3V_{dc}=60V$; $V_{1l}=V_{2l}=V_{3l}=V_{4l}=V_{dc}=20V$ for the thirty-three level inverter with a peak magnitude of 320V, $V_{1u}=V_{2u}=V_{3u}=V_{4u}=V_{5u}=3V_{dc}=48V$; and $V_{1l}=V_{2l}=V_{3l}=V_{4l}=V_{5u}=V_{dc}=16V$ for the forty one level inverter with a peak magnitude of 320V." The proposed multilevel inverters ' simulated results (both output voltage and current) are shown in figure 5 for R=100Ω, L=25mH.

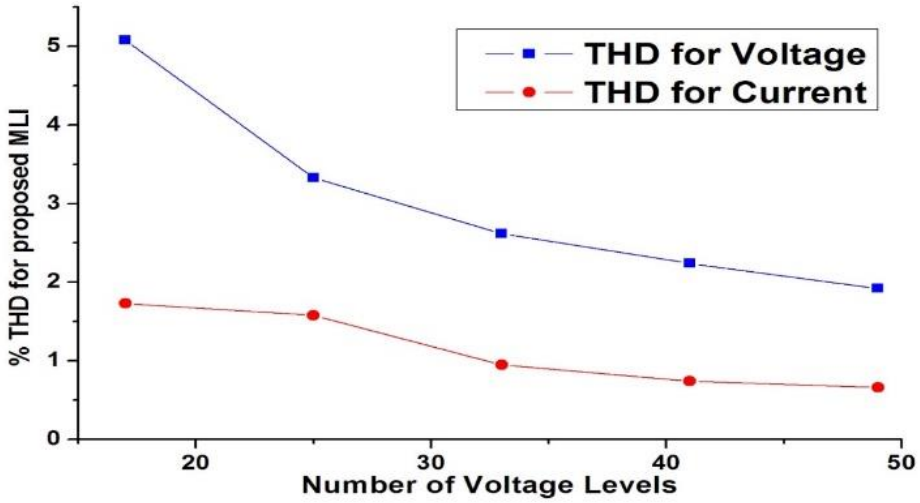


Figure 6. Variation of THD with output levels.

Table 4. Calculated powers and efficiency of the proposed multilevel inverter

Proposed multilevel inverter	Conduction Loss (P_{con}) (W)	Switching loss (P_{sw}) (W)	Output Power (P_{out}) (W)	Intput Power (P_{in}= P_{out}+ P_{con}+P_{sw}) (W)	Efficiency [(P_{out}/P_{in})*100] %
17 level MLI	7.233	0.030	496	503.263	98.55
25 level MLI	8.680	0.031	243	251.711	96.53
33 level MLI	10.127	0.032	272	282.159	96.39
41 level MLI	11.573	0.033	272	283.606	95.90

Total harmonic distortion (THD) for the proposed multilevel inverter for different levels of output is shown in Figure 6. The THD percentage is less than 8% for both current and voltage; hence, as per IEEE519 (Samadaei et al., 2018; Paul et al., 2022), no proposed inverters require no filter circuit.

DOI: https://doi.org/10.52756/ijerr.2023.v36.031

Efficiency and losses in proposed multilevel inverter

The proposed inverter's efficiency is calculated by calculating the output and input power ratio, as illustrated in Table 4. Conduction and switching losses for each level of output have been calculated based on available literature (Samadaei et al., 2016 and 2019; Alishah et al., 2017; Saeedian et al., 2017; Avanaki et al., 2019; Lee, 2018; Dhanamjayulu et al., 2022) and values are noted in the Table 4.

Conclusion

This study introduces a novel multilevel topology capable of generating 17 levels using only nine power switches. This unique design can be easily expanded to accommodate any desired voltage levels. Furthermore, the topology can be categorized into different algorithms based on the availability of DC sources. To validate the effectiveness of the proposed inverter, a prototype model was developed using the A1 algorithm. Extensive analysis of the output voltage and current results confirmed the superior performance of the proposed topology when subjected to RL-load conditions. A comprehensive comparison was conducted between the proposed topology and various recent multilevel inverter topologies. The results clearly indicated that the proposed topology outperforms the others in terms of fewer power electronic devices, cost-effectiveness, simplified circuits, ease of control, high efficiency, lower maintenance requirements, and reduced space utilization. Additionally, the topology operates without the need for filters in accordance with IEEE519 standards. Therefore, based on these findings, it can be concluded that the proposed reduced-switch multilevel inverter is superior to the newly proposed multilevel inverters.

Conflict of interest

There is no conflict of interest to disclose.

References

Abu-rub, H., Member, S., Holtz, J., Rodriguez, J., & Baoming, G. (2010). Medium-Voltage Multilevel Converter-State of the Industrial Applications, *IEEE Transactions on Industrial Electronics*, *57*(8), 2581–2596. https://doi.org/10.1109/TIE.2010.2043039

Alishah, R. S., Hosseini, S. H., Babaei, E., & Sabahi, M. (2017). Optimal Design of New Cascaded Switch-Ladder Multilevel Inverter Structure. *IEEE Trans. Ind. Electron.*, *64*(3), 2072–2080. https://doi.org/10.1109/TIE.2016.2627019.

Alishah, R. S., Hosseini, S. H., Babaei, E., & Sabahi, M. (2016). A New General Multilevel Converter Topology Based on Cascaded Connection of Submultilevel Units with Reduced Switching Components, DC Sources, and Blocked Voltage by Switches. *IEEE Trans. Ind. Electron.*, *63*(11), 7157–7164. https://doi.org/10.1109/TIE.2016.2592460.

Alishah, S. R., Hosseini, S. H., Babaei, E., & Sabahi, M. (2017). Optimization Assessment of A New Extended Multilevel Converter Topology. *IEEE Transactions on Industrial Electronics*, *64*(6), 4530–4538. https://doi.org/10.1109/TIE.2017.2669885

Agrawal, R., &. Jain, S. (2017). Comparison of reduced part count multilevel inverters (RPC-MLIs) for integration to the grid. *Int. J. Electr. Power Energy Syst.*, *84*, 214–224. https://doi.org/10.1016/j.ijepes.2016.05.011.

Ajami, A., Jannati Oskuee, M. R., Mokhberdoran, A., & Van den Bossche, A. (2014). Developed cascaded multilevel inverter topology to minimise the number of circuit devices and voltage stresses of switches. *IET Power Electron.*, *7*(2), 459–466. https://doi.org/10.1049/iet-pel.2013.0080.

Avanaki, H. N., Barzegarkhoo, R., Zamiri, E., Yang, Y., & Blaabjerg, F. (2019). Reduced switch count structure for symmetric multilevel inverters with a novel switched-DC-source submodule. *IET Power Electronics*, *12*(2), 311–321.

Arun, N., & Noel, M. M. (2018). Crisscross switched multilevel inverter using cascaded semi-half-bridge cells. *IET Power Electron.*, *11*(1), 23–32, 2018. https://doi.org/10.1049/iet-pel.2016.0644.

Ahrabi, R., Farakhor, A., Najafi Ravadanegh, S., & Ardi, H. (2015). Symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components. *IET Power Electron.*, *8*(6), 1052–1060. https://doi.org/10.1049/iet-pel.2014.0378.

Carpita, M., Moser, D., Marchesoni, M. & Pellerin, M. (2008). Multilevel converter for traction applications: Small-scale prototype tests results. *IEEE Trans. Ind. Electron.*, *55*(5), 2203–2212. https://doi.org/10.1109/TIE.2008.918645.

Dahidah, M. S. A., Konstantinou, G., & Agelidis, V. G. (2015). A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications. *IEEE Trans. Power Electron.*, *30*(8), 4091–4106. https://doi.org/10.1109/TPEL.2014.2355226.

Dhanamjayulu, C., Rudravaram, V., & Kumar, S. P. (2022). Design and implementation of a novel 35-level inverter topology with reduced switch count. *Electric Power Systems Research*, *212*, 108641. https://doi.org/10.1016/j.epsr.2022.108641

Franquelo, L. G., J. Rodriguez, J., Leon, J. I., Kouro, S., Portillo, R., & Prats, M. M. (2008). The age of multilevel converters arrives. *IEEE Ind. Electron. Mag*., *2*(2), 28–39, 2008. https://doi.org/10.1109/MIE.2008.923519.

Gautam, S. P., Gupta, S., & Sahu, L. K. (2016). Reduction in number of devices for symmetrical and asymmetrical multilevel inverters. *IET Power Electron*., *9*(4), 698–709. https://doi.org/10.1049/iet-pel.2015.0176.

Gautam, S. P., Kumar, L., & Gupta, S. (2018). Single-phase multilevel inverter topologies with self-voltage balancing capabilities. *IET Power Electron*., *11*(5), 844–855. https://doi.org/10.1049/iet-pel.2017.0401.

Jha, K. K., Mahato, B., Prakash, P., & Jana, K. C. (2016). Hardware implementation of single phase power factor correction system using micro-controller. *Int. J. Power Electron. Drive Syst.*, *7*(3), 790–799. https://doi.org/10.11591/ijpeds.v7.i3.pp790-799.

Kumar, C., Mahato, B., Raushan, R., Maity, T., & Jana, K. C. (2016). Comprehensive Study of various configurations of three-phase Multilevel inverter for different levels. *3rd Int'l Conf. on Recent Advances in Information Technology I RAIT-2016I*, 310-315. https://doi.org/10.1109/RAIT.2016.7507922.

Kumar, V.A.G., & Reddy, D. M. (2023). TLBO-trained ANN-based Shunt Active Power Filter for Mitigation of Current Harmonics. *International Journal of Experimental Research and Review*, *34*(Special Vo), 11-21. https://doi.org/10.52756/ijerr.2023.v34spl.002

Lee, S. S. (2018). Single-Stage Switched-Capacitor Module (S3CM) Topology for Cascaded Multilevel Inverter. *IEEE Transactions on Power Electronics*, *33*(10), 8204–8207. https://doi.org/10.1109/TPEL.2018.2805685

Mahato, B., Majumdar, S., & Jana, K. C. (2018). Carrier-Based PWM Techniques for Multi-Level Inverters: A Comprehensive Performance Study. *J. Sci. PART A Eng. Innov*., *5*(3), 101–111.

Mahato, B., Raushan, R., & Jana, K. C. (2016). Comparative Study of Asymmetrical Configuration of Multilevel Inverter for Different Levels, 3rd International Conference on Recent Advances in Information Technology (RAIT), 300–303. https://doi.org/10.1109/RAIT.2016.7507920

Mahato, B., Mittal, S., Majumdar, S., Jana, K. C., & Nayak, P. K. (2019). Multilevel Inverter with Optimal Reduction of Power Semi-conductor Switches. Renewable Energy and its Innovative Technologies, Springer Singapore, 31–50.

Mahato, B., Raushan, R., & Jana, K. C. (2017). Modulation and control of multilevel inverter for an open-end winding induction motor with constant voltage levels and harmonics. *IET Power Electron.*, *10*(1), 71–79. https://doi.org/10.1049/iet-pel.2016.0105.

Mahato, B., Jana, K. C. & Thakura, P. R. (2018). Constant V / f Control and Frequency Control of Isolated Winding Induction Motor Using Nine-Level Three-Phase Inverter. *Iran. J. Sci. Technol. Trans. Electr. Eng*., *6*(1), 1–13. https://doi.org/10.1007/s40998-018-0064- 6.

Malekjamshidi, Z., Jafari, M., Islam, R., Zhu, J., & Member, S. (2014). A Comparative Study on Characteristics of Major Topologies of Voltage Source Multilevel Inverters. *2014 IEEE Innovative Smart Grid Technologies-Asia* (ISGT ASIA), pp. 612-617. https://doi.org/10.1109/ISGT-Asia.2014.6873862

Mukherjee, A., Mahato, B., Sinha, A., & Jana, K. C. (2017). Comparative performance analysis of PV based grid-tied single phase asymmetrical multilevel inverter using different PWM techniques. *J. Electr. Eng*., *17*(1) 132-141.

Meshram, P. M., & Borghate, V. B. (2015). A simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC). *IEEE Trans. Power Electron.*, *30*(1), 450–462. https://doi.org/10.1109/TPEL.2014.2317705

Nanda, L., Dasgupta, A., & Rout, U. K. (2017). Hybrid Symmetrical Cascaded Multilevel Inverter having reduced number of Switches and DC Sources. *International Journal of Applied Engineering Research*, *12*(15), 5151-5155.

Naderi, R., & Rahmati, A. (2008). Phase-shifted carrier PWM technique for general cascaded inverters. *IEEE Trans. Power Electron*., *23*(3), 1257–1269. https://doi.org/10.1109/TPEL.2008.921186.

Omer, P., Kumar, J., & Surjan, B. S. (2018). A New Multilevel Inverter Topology with Reduced Switch Count and Device Stress, *2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON)*, Gorakhpur, India, pp. 1-6. https://doi.org/10.1109/UPCON.2018.8596999.

Paul, S., Jana, K. C., Majumdar, S., Pal, P. K., & Mahato, B. (2022). Performance Analysis of a Multi-module Staircase (MM-STC) Type Multilevel Inverter with Reduced Component Count and Improved Efficiency. *IEEE Journal of Emerging and*

Selected Topics in Power Electronics, *10*(6), 6619-6633. https://doi.org/10.1109/JESTPE.2021.3133346

Rodriguez, J., Bernet, S., Steimer, P. K., & Lizama, I. E. (2010). A Survey on Neutral Point- Clamped Inverters. *IEEE Trans. Ind. Electron*., *57*(7), 2219–2230. https://doi.org/10.1109/TIE.2009.2032430.

Raushan, R., Mahato, B., & Jana, K. C. (2018). Optimum structure of a generalized three-phase reduced switch multilevel inverter. *Electr. Power Syst. Res*., *157*, 10–19. https://doi.org/10.1016/j.epsr.2017.11.017.

Rashid, M. H. (2004). Power electronics: Circuits, devices and application.

Rodríguez, J., Lai, J. S., & Peng, F. Z. (2002). Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron*., *49*(4), 724–738. https://doi.org/10.1109/TIE.2002.801052.

Rodríguez, J., Bernet, S., Wu, B., Pontt, J. O., & Kouro, S. (2007). Multilevel voltage-source-converter topologies for industrial medium-voltage drives, *IEEE Trans. Ind. Electron*., *54*(6), 2930–2945. https://doi.org/10.1109/TIE.2007.907044.

Samadaei, E., Sheikholeslami, A., Gholamian, S. A., & Adabi, J. (2018). A Square T-Type (ST- Type) Module for Asymmetrical Multilevel Inverters. *IEEE Trans. Power Electron*., *33*(2), 987–996. https://doi.org/10.1109/TPEL.2017.2675381.

Saeedian, M., Adabi, J., & Hosseini, S. M. (2017). Cascaded multilevel inverter based on symmetric–asymmetric DC sources with reduced number of components. *IET Power Electronics*, *10*(12), 1468–1478.

Samadaei, E., Gholamian, S. A., Sheikholeslami, A., & Adabi, J. (2016). An Envelope Type (E-Type) Module: Asymmetric Multilevel Inverters with Reduced Components, *IEEE Trans. Ind. Electron*., *63*(11), 7148–7156. https://doi.org/10.1109/TIE.2016.2520913.

Samadaei, E., Kaviani, M., & Bertilsson, K. (2019). A 13-levels module (KType) with two DC sources for multilevel inverters. *IEEE Transactionson Industrial Electronics*, *66*(7), 5186–5196.

Sumit, R. A., & Kumar, S. (2021). A novel generalised topology of a reduced part count multilevel inverter with level boosting network to improve the quality of supply. *Global Transitions Proceedings*, *2*(2), 238-245. https://doi.org/10.1016/j.gltp.2021.08.019

Tolbert, L. M., Peng, F. Z., & Habetler T. G. (1999). Multilevel converters for large electric drives. *IEEE Trans. Ind. Appl*., *35*(1), 36–44. https://doi.org/10.1109/28.740843

How to cite this Article:

Samrat Paul, Sourav Debnath, Dipak Kumar Mandal and Bidyut Mahato (2023). A Modified 17-level H-Type Inverter Topology with Optimal Reduction of Power Electronic Components. *International Journal of Experimental Research and Review*, *36*, 347-358.

DOI : https://doi.org/10.52756/ijerr.2023.v36.031

This work is licensed under a Creative Commons Attribution-NonCommercial-NoDerivatives 4.0 International License.