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Meta Heuristic Algorithm Based Novel Dstatcom Architecture for Power Quality Improvement

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Abstract: Electric utility systems are increasingly favoured as local energy systems due to their ability to integrate renewable energy, improve energy efficiency, and enhance the resilience of the power grid. However, while these benefits are significant, they also present certain complexities related to control and power quality (PQ). PQ is crucial within utility systems to ensure the proper functioning of connected devices and the overall health of the system. Therefore, both voltage quality and current quality are of utmost importance. Control strategies combined with advanced power electronics devices (PED) provide a robust framework to address PQ challenges. This paper introduces a novel approach for constructing a distributed Static Synchronous Compensator (DSTATCOM) utilizing innovative 125-level asymmetric multilevel DC link inverters to enable multilevel operation. A modified 125-level multilevel inverter aimed at enhancing power quality is proposed herein. By employing a minimal number of components, this inverter can generate 125-level voltages per phase, serving as a DSTATCOM to address power quality issues such as sag, swell, and harmonics. Bidirectional DC-DC converters are employed for purposes other than just providing power to the inverter's DC connections replacing DC sources. Additionally, the Coati Optimization Algorithm (COA), a newly introduced metaheuristic approach inspired by observed behavioural patterns in coatis in their natural habitat, is presented. COA is designed to emulate two primary behaviours of coatis: (i) their hunting strategy when pursuing iguanas and (ii) their evasion tactics when confronted by predators. To validate the effectiveness of the Coati Optimization algorithm, simulation is carried out with Matlab Simulink, and the outcomes of the simulation for the proposed scheme are provided in this paper. The efficacy of Solar-PV integrated 125-level asymmetric multilevel DC link inverter in enhancing power quality by adhering to the IEEE-519 Standards is demonstrated.

Introduction

Over the past few decades, multilevel inverters have become more and more important. Because these new inverters can provide waveforms with an improved harmonic spectrum and reduced THD, they are appropriate for elevated voltage and distributed power applications. Two of the biggest issues in power production, transmission, and distribution systems are power grid volatility and power quality. These issues typically originate from improper power flow management. Linking nonlinear, unsteady, or reactive loads to the grid may lead to voltage-related challenges, including sags/swells, imbalance, oscillations, high harmonic content, transients, and a low power factor (Trabelsi et al., 2021; Vemuganti et al., 2021). The integration of both non-renewable and renewable energy sources into distributed power generation systems has further exacerbated instability and power quality issues.

A variety of flexible AC transmission system (FACTS) controllers are presently being explored and documented in the literature (Chethan and Kuppan, 2024; Arockiaraj et al., 2023), aiming to mitigate these issues. These controllers are typically classified into two main categories: thyristor-based and Voltage Source Inverter

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(VSI)-based FACTS controllers. VSI-based controllers encompass Static Synchronous Compensators (STATCOM), Static Synchronous Series Compensators (SSSC), and Unified Power Flow Controllers (UPFC) (Kar et al., 2020; Hingorani and Gyugyi, 2000).

As one of the most adaptable and powerful FACTS controllers for managing power flow, controlling grid voltages, and increasing efficiency, multilevel VSI-based compensating devices are regarded as superior (Umadevi et al., 2024). Multilevel inverters have several benefits over conventional two-level VSIs, including lower harmonic distortion, higher AC voltage levels, less voltage stress on electrical devices, lower switching frequency operating, and good reliability. Multilevel inverters have grown crucial in medium- and high-power applications because of these qualities (Chakrabarty and Adda, 2021; Duarte et al., 2022).

A novel 125 multilevel Asymmetric architecture appropriate for STATCOM applications is presented in this research. However, since the STATCOM does not require active power, solar DC-DC converters are utilized in this study in place of the DC sources, significantly reducing the cost. Since the asymmetric multilevel inverter (AMLI) can synthesize additional voltage levels of output with the same number of components, it is a very appealing topology for power quality issues. The proposed Multilevel STATCOM replaces the conventional approach with a meta-heuristic Coati optimization algorithm, allowing it to function with conventional modulation methods such as sinusoidal PWM. It has lately gained popularity as a high-voltage solution for uses including energy storage systems (Gultekin and Ermiş, 2013; Marzo et al., 2022), static synchronous compensators (STATCOM) (Jung et al., 2018; Ajayi-Obe, 2023; Michail and Alfred, 2015).

Proposed Topology

According to (NV, 2023), The multilayered DC link inverter (MLDCL) stands out as one of the extensively employed topologies for reduced switch multilevel inverter (MLI) configurations. Depending on the number of output levels, various DC sources are required for this independent type MLI (Agrawal and Jain, 2017), Asymmetrical configurations require fewer switching devices and sources of electricity than symmetrical configurations for the same output voltage levels.

The MLI design depicted in Figure 1 consists of the Polarity generation circuit, distinguished by its asymmetric fundamental circuit, and the Level generator unit, which incorporates an H-bridge inverter circuit, forming the complete structure (Vijeh et al., 2019). It is noteworthy that the toggle switches within the polarity generation circuit experience greater stress compared to their counterparts in the level generation unit. A phase for polarity generation plus a phase for level generation make up MLDCL, a hybrid variant of MLI. Figure 1 displays a schematic structure illustrating the 125- level inverter output.

The triggering circuit's control signals govern both the Level Generation Circuitry and the Polarity Generation Circuit. Asymmetric arrangements can achieve higher output levels for a comparable quantity of semiconductor components and voltage sources than their symmetric counterparts.

Figure 1 depicts the MLDCL inverter structure, which has six DC sources. A stair-step waveform representing positive and zero magnitudes of voltage is produced by the level-producing stage. The output of the H-Bridge-based polarity generating stage, on the other hand, resembles a sine wave since it alternatively inverts every second's half-cycle of the waveform created by the level production phase hooked on negative levels (Abdalla et al., 2016). Utilizing the identical configuration as depicted in Figure 2, 125 levels of output voltage are produced through an asymmetrical DC supply configuration. The determination of DC sources for these 125 output levels is achieved through a combination of geometric progression and the binary approach, as outlined in (Gupta et al., 2016).

$$V_6=2V_5=2V4 = 2V3 = 2V2 = 2V \quad (1)$$

In contrast to a symmetrical setup, the number of switches and levels needed for an asymmetrical Multilayered DC Link (MLDCL) inverter can be described in a generalized manner, as indicated in (Venkataramanaiah et al., 2017)

$$N_{L,asym} = 2n + 1, \quad (2)$$

$$N_{S,asym} = 2n + 4 \quad (3)$$

The foundation of this design is established through the series coupling of one-stage sub-multilevel converter modules with a full bridge stacked H-bridge inverter. The primary aim of this article is to enhance the output voltage depicted in Figure 1 by incorporating additional levels while minimizing the use of switches. To create the 125-level single-phase output voltage observed in nature, 6 uneven voltage sources (V1, V2, V3, V4, V5, and V6) and 12 unilateral switches (S1, S2, S3, S4....S12) using an IGBT and antiparallel diode combination were needed.

The MLDCL inverter is the best option for integrating PV systems because of its ability to quickly replace isolated DC sources. As seen in Figure 2, the integration entails connecting PV panels and inverters via a bidirectional DC-DC converter. Before putting the output level produced by the DC-DC converters into the inverter in this process, it is imperative to determine whether it is suitable. However, changes in ambient temperature and solar irradiation, both of which occur over time, can affect how well PV panels operate.

Through the use of a DC-DC Flyback converter, the Bidirectional DC-DC Converter increases the output voltage produced by PV panels, allowing it to provide AMLI with varying voltages between V1 and V6. The Flyback converter (FBC) and switch-mode DC power supply (SMPS) with R load are shown in Figure 3. When the operating switch is turned on, the FBC transfers energy from the main circuit to the other side by use of its built-in polarity inductance. Snubber circuits are incorporated with the switches to reduce voltage spikes that occur during switch-off.

Figure 4 illustrates the improvement in the performance of the flyback DC-DC converter achieved by providing asymmetric voltage outputs to the inverter. These varying voltage levels serve as DC link modules for half-bridge devices connected in series. Drawing inspiration from natural processes, the Coati Optimization Algorithm generates pulses for the inverter and its 125-level output is shown in Figure 5.

Coati Optimization Technique

The Coati Optimization Algorithm (COA) is a newly developed metaheuristic algorithm inspired by the behaviours of coatis; intelligent mammals recognized for their forest-foraging habits. The algorithm has been presented to solve optimization problems by simulating the communal foraging behaviour of coatis. To create a successful optimization process, COA imitates the communal actions of coatis, including their food-searching and group-coordination strategies.

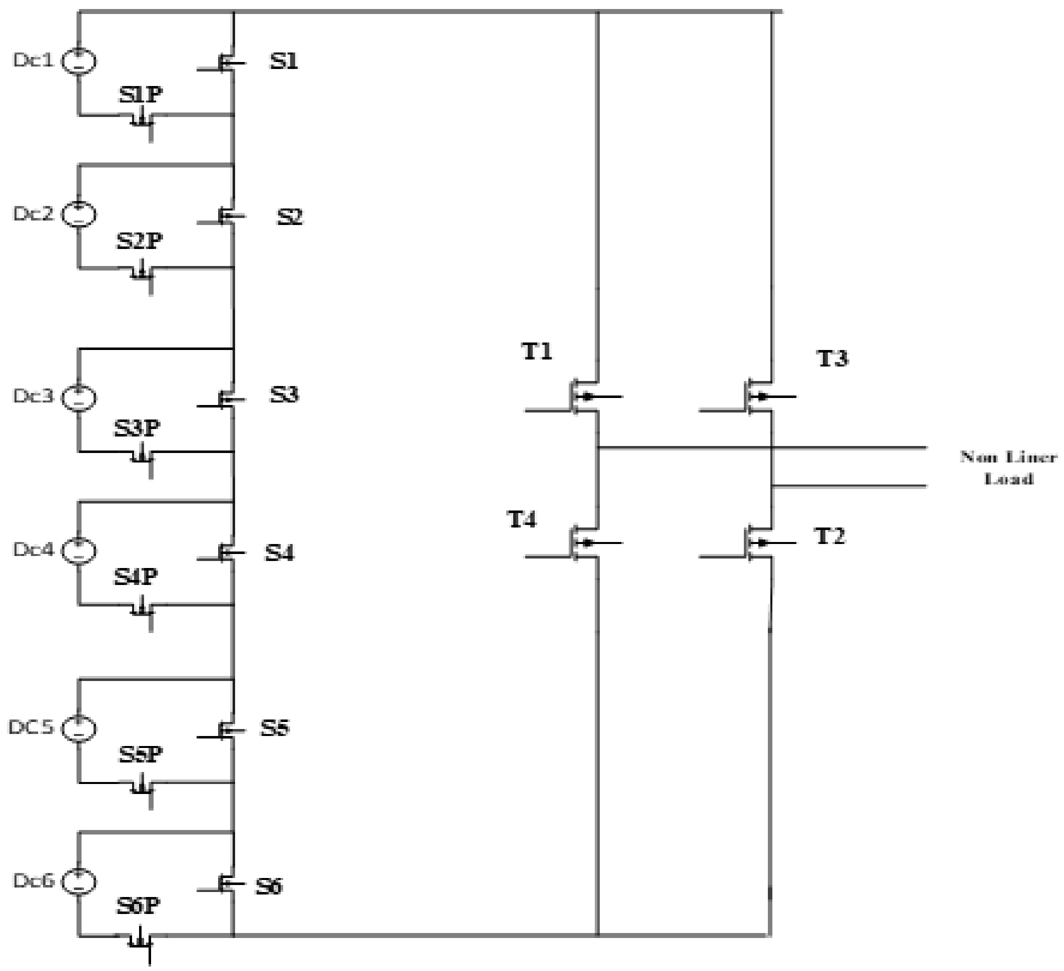

Figure 1. Proposed 125-level MLDCL Inverter

COA has been applied to a wide range of optimization issues in science, engineering, and technology. To discover the best answers, it makes use of the investigation and utilization of traits found in coatis' foraging activity. The COA seeks to strike an equitable compromise between global and local search abilities by striking a balance between exploration and exploitation, which could make it useful in resolving challenging optimization issues.

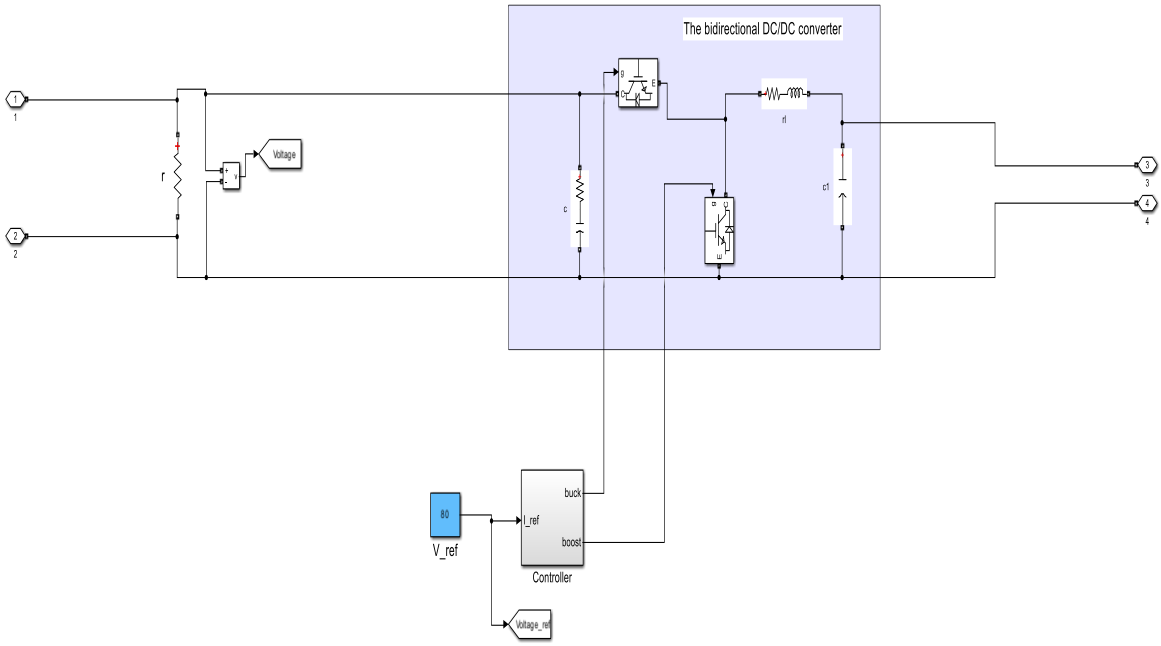

Figure 2. Bidirectional DC-DC Converter.

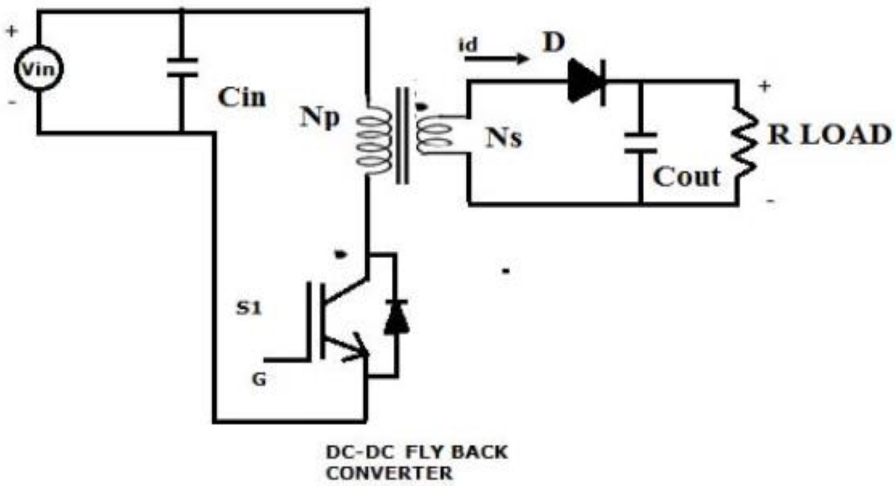

Figure 3. DC-DC Flyback Converter.

Figure. 6 displays an illustration of a coati. As omnivores, coatis consume both invertebrates like tarantulas and tiny vertebrate prey like lizards, rodents, alligator eggs, and bird eggs. A green iguana seems to be one of Coati’s favourite snacks. Coatis chase iguanas in bunches because they are huge reptiles that are frequently seen in trees. While certain individuals quickly launch an attack on the iguana, others climb trees to startle it, prompting it to leap to the ground. Nevertheless, coatis

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are vulnerable to predator attacks. Maned wolves, anacondas, foxes, boa constrictors, tayras, dogs, jaguarundis, and ocelots are among the predators that hunt coatis. Large raptors like ornate harpy eagles, hawk eagles and black-and-chestnut eagles, also hunt them (Dehghani et al., 2023).

The strategies Coatis employ in confronting iguanas and their responses when encountering and avoiding predators exemplify sophisticated behaviours. The suggested COA technique was designed mostly with inspiration from the simulation aforementioned natural coatis' actions. This study is innovative because it

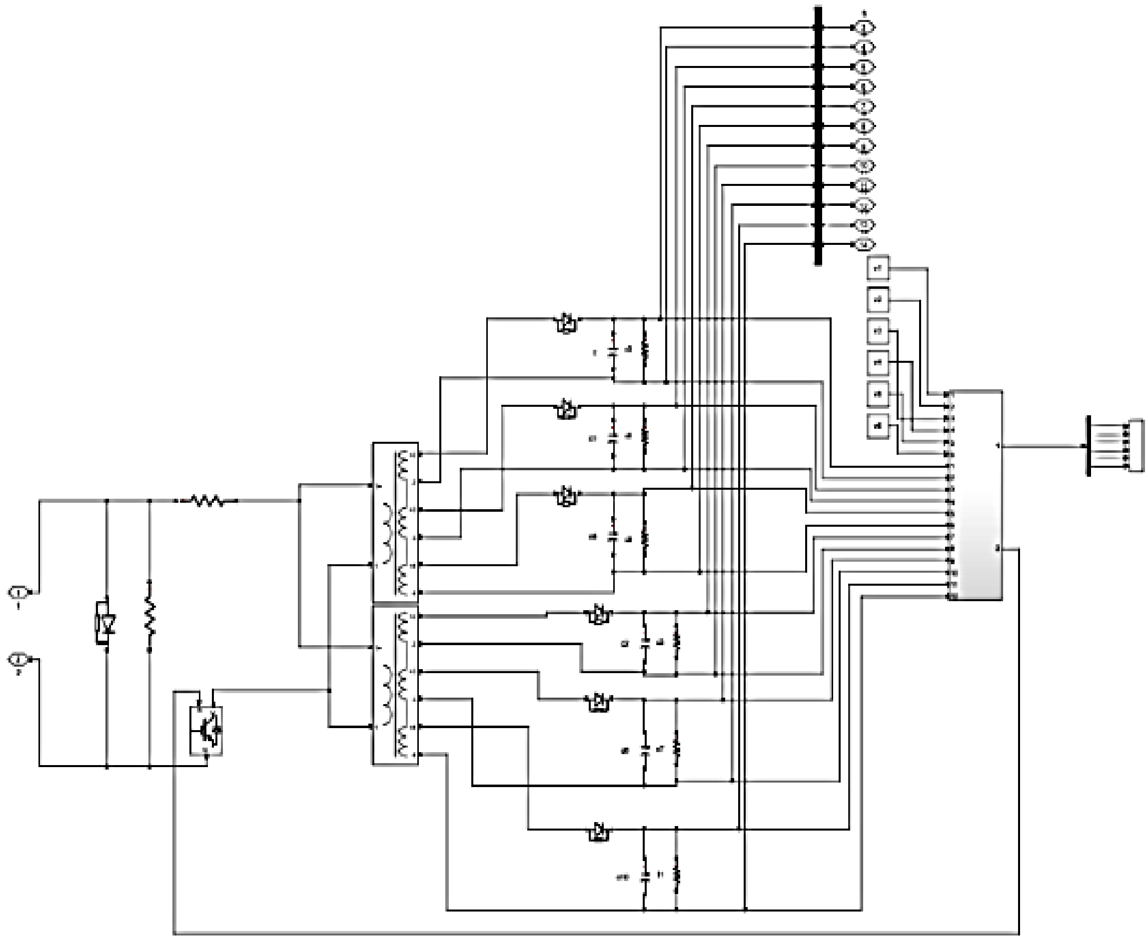

Figure 4. DC-DC Flyback converter with Multi-Output.

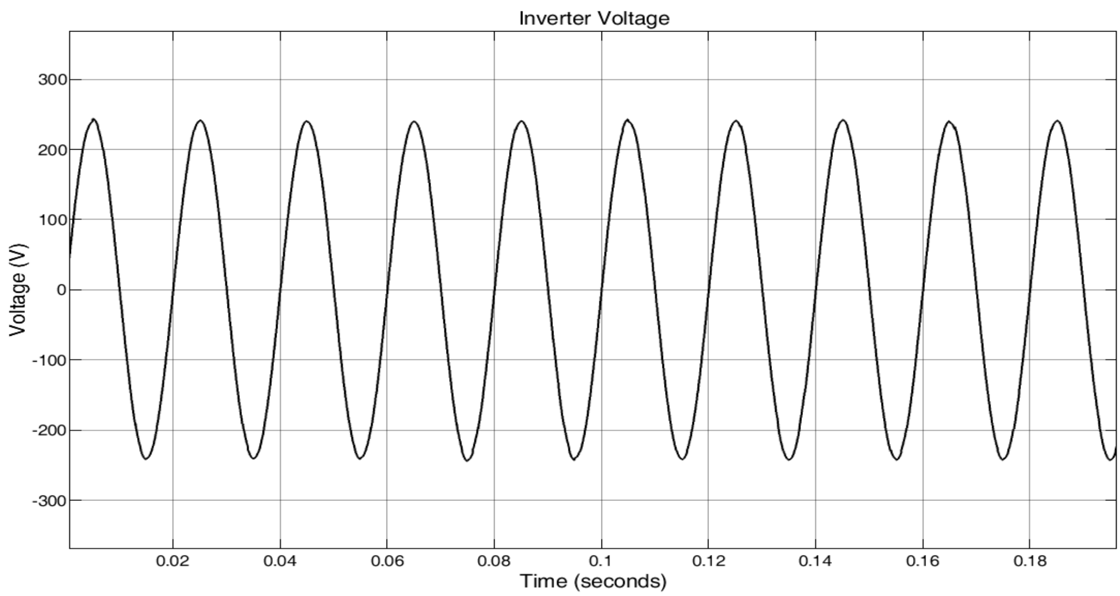

Figure 5. Proposed Inverter Output.

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presents the Coati Optimization technique (COA), a new optimization technique that can be used to generate switching pulses to an asymmetric multilevel inverter which is used as a Dstatcom for power quality improvement. The proper gate pulses must be generated in multilevel inverters to minimize harmonic distortion and produce superior output voltage waveforms.

The Coati Optimization technique (COA) can be used to generate these. By maximizing the multilayer inverter's switching patterns, the POA can minimize the total number of switching transitions, minimize the voltage's total harmonic distortion (THD) at its output, and maximize power conversion efficiency. The COA can help determine the optimal switching angles and sequences for the various voltage levels of the multilevel inverter.

Figure 6. An image of a Coati during a hunt.

Two of coatis' natural activities are modelled in order to update the location of coatis (possible solutions) in the COA. Among these actions are:

(i) The coatis's attack approach against iguanas;

(ii) The coatis's method of escaping from predators.

Consequently, these are two distinct phases of updating the COA population.

Phase 1: The approach for hunting and attacking iguanas (exploration phase).

To update the coati's community in the search space, their first attack method on iguanas is modelled. This strategy entails a group of coatis climbing a tree to approach an iguana and induce fear. Upon the iguana's descent to the ground, additional Coatis gather beneath a tree. Subsequently, the coatis hunt and assail the iguana post-landing. This approach leads to coatis migrating to diverse locations within the search field, illustrating the COA's capability for extensive exploration in the global search within the problem-solving domain. Figure 7 depicts the pattern diagram for this tactic.

In the COA design, the iguana assumes the role of the most coveted member of the population. Furthermore, it is postulated that fifty percent of the coatis climb the tree, while the remaining half waits patiently for the iguana to descend.

Consequently, the numerical simulation of the coatis' positions upon descending from the tree is conducted using Equation (4).

$$X_i^{P_1}: x_{i,j}^{P_1} = x_{i,j} + r \cdot \left(Iguana_j - I \cdot x_{i,j}\right),$$
$$fori = 1,2, \ldots\ldots, \left[\frac{N}{2}\right] and$$
$$j = 1,2, \ldots\ldots m. \quad (4)$$

The iguana is released to the ground and subsequently placed randomly within the search area. Coatis on the ground traverse the search space, as simulated by Equations (5) and (6), based on this randomly assigned position.

$$Iguana^G: Iguana_j^G = lb_j + r \cdot (ub_j - lb_j),$$
$$j = 1,2, \ldots\ldots\ldots m \quad (5)$$

$$X_i^{P1}: x_{i,j}^{P1} = \begin{cases} X_{i,j} + r \cdot (Iguana_j^G - I \cdot x_{i,j}), & F_{Iguana^G} < F_i \\ x_{i,j} + r \cdot (x_{i,j} - Iguana_j^G), & else, \end{cases} \quad (6)$$

For i= $[\frac{N}{2}] + 1, [\frac{N}{2}] + 2, \ldots\ldots. N \ and \ j = 1,2, \ldots\ldots m$

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Should the updated position of each coati amplify the importance of the objective function, the coati remains in its initial position; otherwise, a new position is computed for each coati. The updating condition for the simulated values of i = 1, 2…., N is expressed as follows in Equation (7).

$$X_i = \begin{cases} X_i^{P1}, & F_i^{P1} < F_i \\ X_i & else. \end{cases} \quad (7)$$

In this context, X_i^{P1} represents the newly computed position for the ith coati, where $x_{i,j}^{P1}$ denotes its jth dimension. F_i^{P1} corresponds to its objective function value, and \(r\) is a random real number within the [0, 1] interval. "Iguana" denotes the position of the best member in the search space, with $Iguana_j$ representing

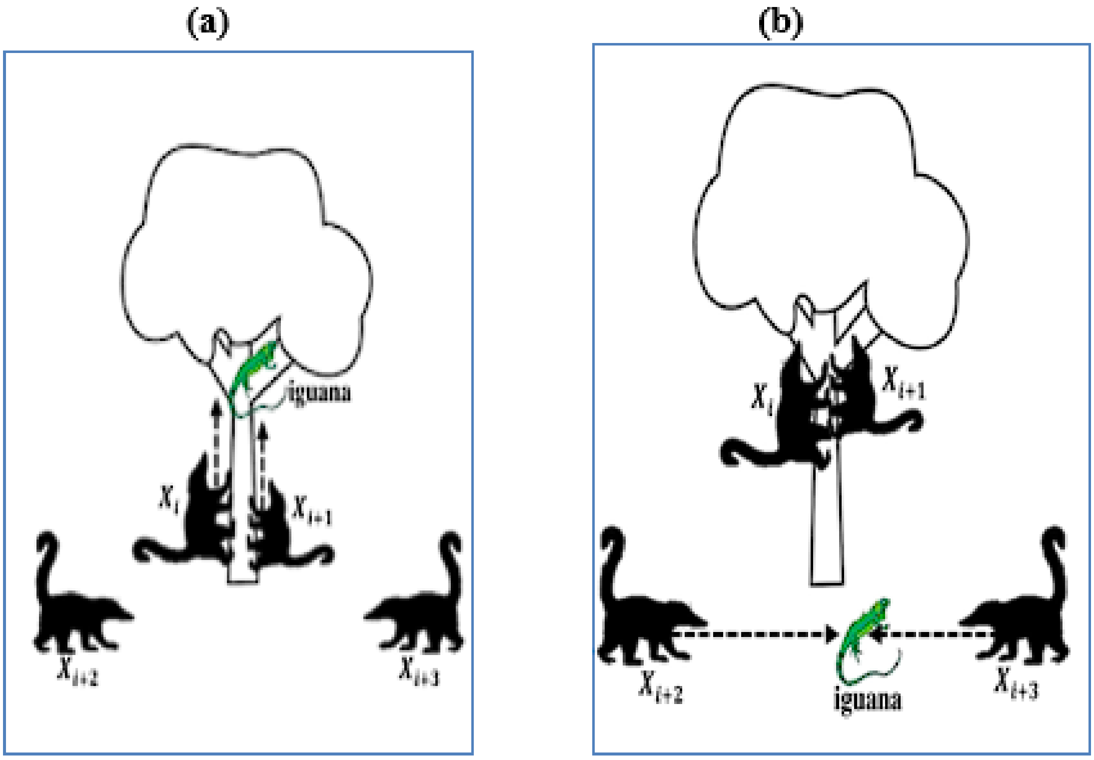

Figure 7. Initial phase of COA pattern diagram. (a) The iguana perched on the tree is attacked by 50% of the coati's population. (b) the remaining half of the coati's population, which goes after fallen iguana on the ground.

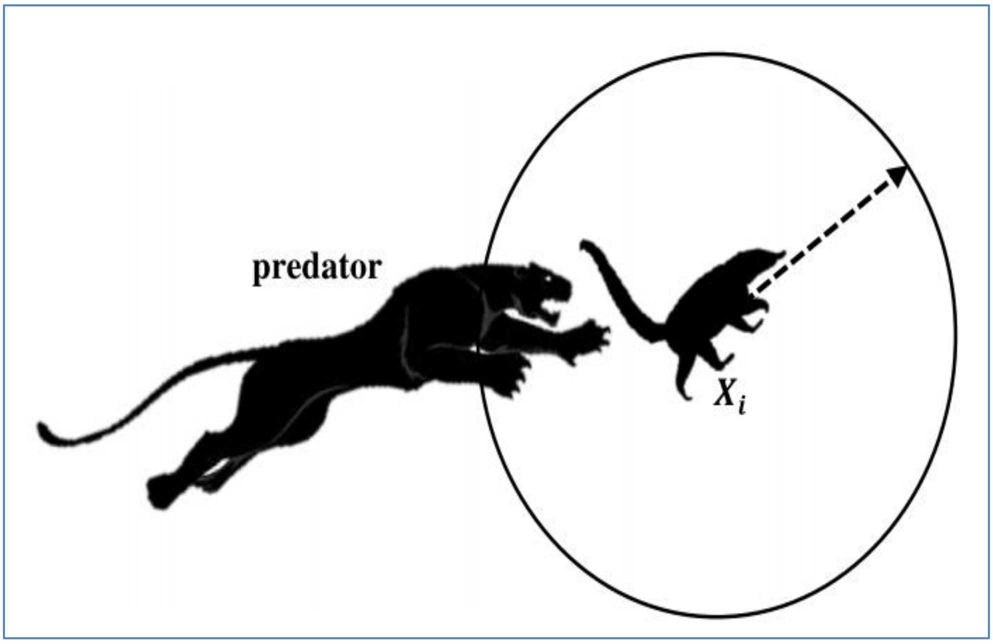

Figure 8. Coati's escape from a predator during the COA Phase II.

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its jth dimension. I is an integer randomly selected from the set {1, 2}, and $Iguana^G$ is the randomly generated position of the iguana on the ground. $Iguana_j^G$ signifies its jth dimension, F_{Iguana^G} is its objective function value, and $\lfloor\cdot\rfloor$ denotes the floor function (also known as the greatest integer function).

Phase 2: The exploitation phase, or the process of running away from predators

Based on how coatis naturally interact with and flee from predators, a mathematical model is used to simulate the second step of the procedure of updating coatis' locations in the search space. When faced with a predator, a coati retreats from its current position. The Coati's actions in this strategy result in it finding a secure location in proximity to its existing position, showcasing the COA's ability for local search exploitation. Figure. 8 shows the pattern diagram for these coatis escape methods from predators. To replicate this pattern of action, an arbitrary position is created using Eqs. in the vicinity of each coati's location. Both (8) and (9).

$$lb_j^{local} = \frac{lb_j}{t}, ub_j^{local} = \frac{ub_j}{t}, \quad where\ t = 1,2,\ldots\ldots..T. \qquad (8)$$

$$X_i^{P2}: x_{i,j}^{P2} = x_{i,j} + (1-2r) \cdot \left(lb_j^{local} + r \cdot \left(ub_j^{local} - lb_j^{local}\right)\right), \qquad (9)$$

$$i = 1,2,\ldots..N, \quad j = 1,2,\ldots\ldots m$$

Should the newly calculated position lead to an increase in the objective function's value, a scenario reflected by this condition and expressed in Equation (10),

$$X_i = \begin{cases} X_i^{P2}, & F_i^{P2} < F_i, \\ X_i, & else, \end{cases} \qquad (10)$$

In this context, X_i^{P2} signifies the newly computed position for the ith coati, determined during the second phase of COA. Here, $x_{i,j}^{P2}$ denotes its jth dimension, and F_i^{P2} represents its objective function value. The variables r and t denote a random number within the [0, 1] interval and the iteration counter, respectively. Additionally, lb_j^{local} and ub_j^{local} stand for the local lower bound and local upper bound of the jth decision variable, while lb_j and ub_j represent the overall lower bound and upper bound of the same decision variable, respectively.

Step by Step procedure for generating gate pulses using Coati Algorithm:

1. **Start**
2. **Initiate the population of pulse patterns randomly within the feasible range.**
3. **Assess the fitness of each pulse pattern using performance metrics (e.g., THD, voltage deviation, power losses, etc.)**
4. **Initialize the iteration counter to 0.**
5. **Continue iterations until a termination condition is reached:**
   a) **Increment the iteration counter.**
   b) **Conduct exploration to locate promising pulse patterns**:

- Adjust the switching times of pulse patterns through random movements.
- Evaluate the fitness of the modified pulse patterns.

   c) **Execute exploitation to refine the best pulse patterns:**

- Share information among pulse patterns to simulate cooperative behaviour.
- Update and refine the pulse patterns based on shared information.
- Evaluate the fitness of the updated pulse patterns.

   d) **Adaptively update the COA parameters based on the performance of the pulse patterns.**

6. **Select the optimal pulse pattern(s) based on the fitness evaluation.**
7. **END.**

Results and Discussion

The proposed PV-enabled Asymmetric multilevel DC link inverter model used as a Dstatcom is simulated in MATLAB 2022b Simulink. The simulation is subsequently conducted to analyse the performance of Non-linear load conditions, Voltage Sag, and Swell situations, employing the proposed algorithm for evaluation. CO algorithm is implemented to generate the gate pulses to a multilevel inverter.

Figure 9 represents the proposed Simulink model. During uncompensated case the Asymmetrical MLI as Dstatcom successfully mitigated the 2.02 per unit (P.U.) swell occurring at t=0.2ms to 0.4ms and the 5.06 P.U. voltage sag occurring at 0.5ms to 0.7ms, restoring the current & voltage to its rated load level as shown in Figure 10 and 13.23 % THD is obtained without compensation.

Simulation has been used to confirm the effectiveness of the 125-level multilevel inverter for minimizing harmonics that was previously reported. To compensate for those swell and sag in grid voltage firstly, proposed asymmetrical multilevel dc link inverter's THD is analysed and is obtained as 0.97% as shown in Figure 11.

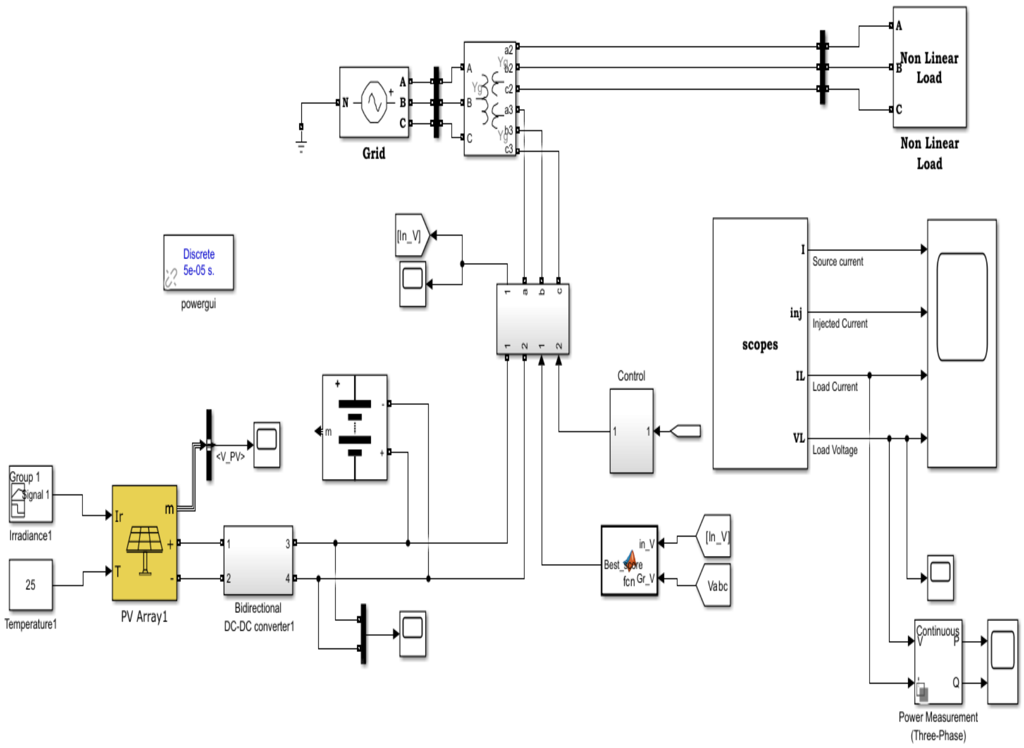

Figure 9. Proposed Simulink Model.

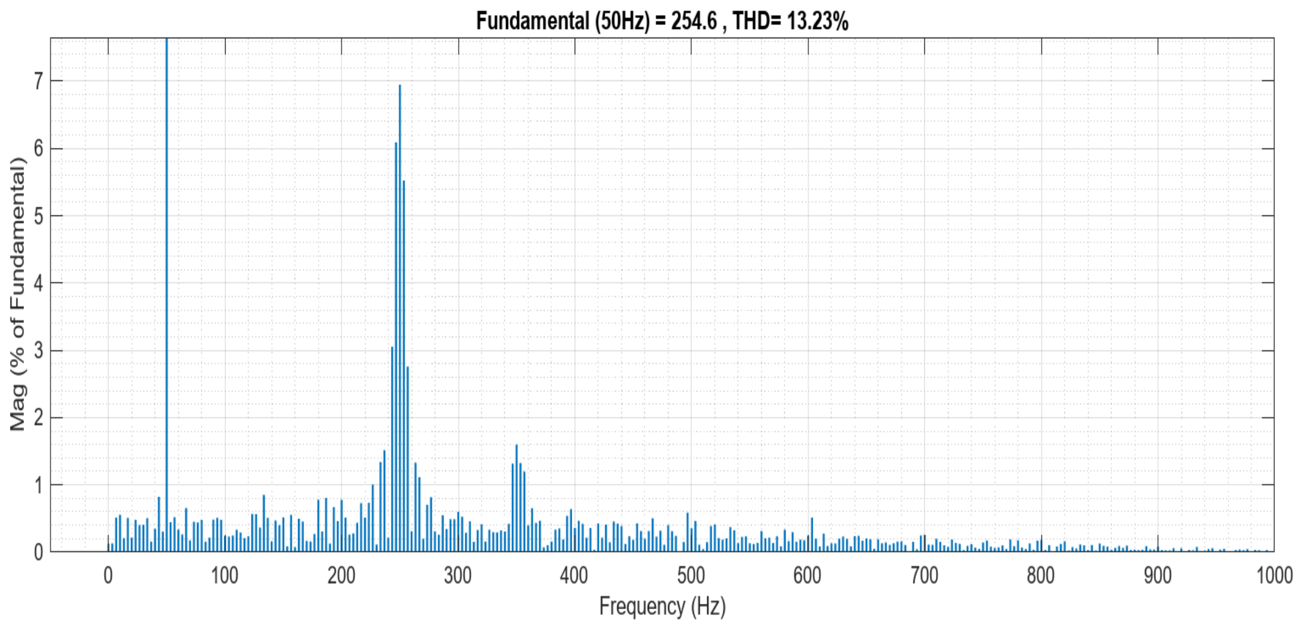

Figure 10. THD analysis without compensation.

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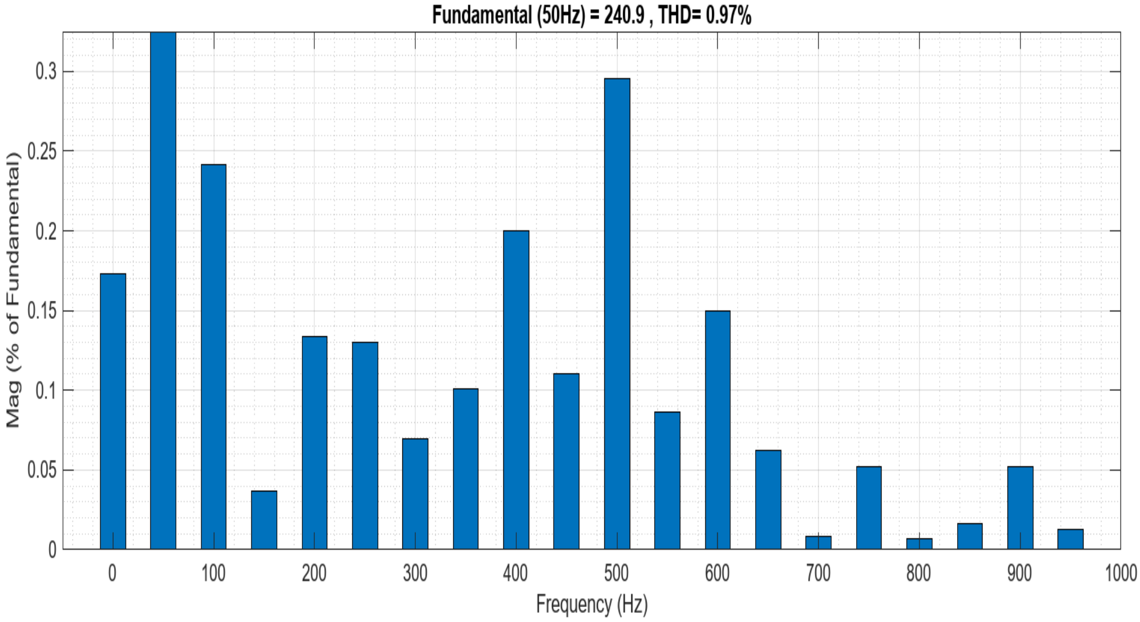

Figure 11. Harmonic analysis of the proposed inverter.

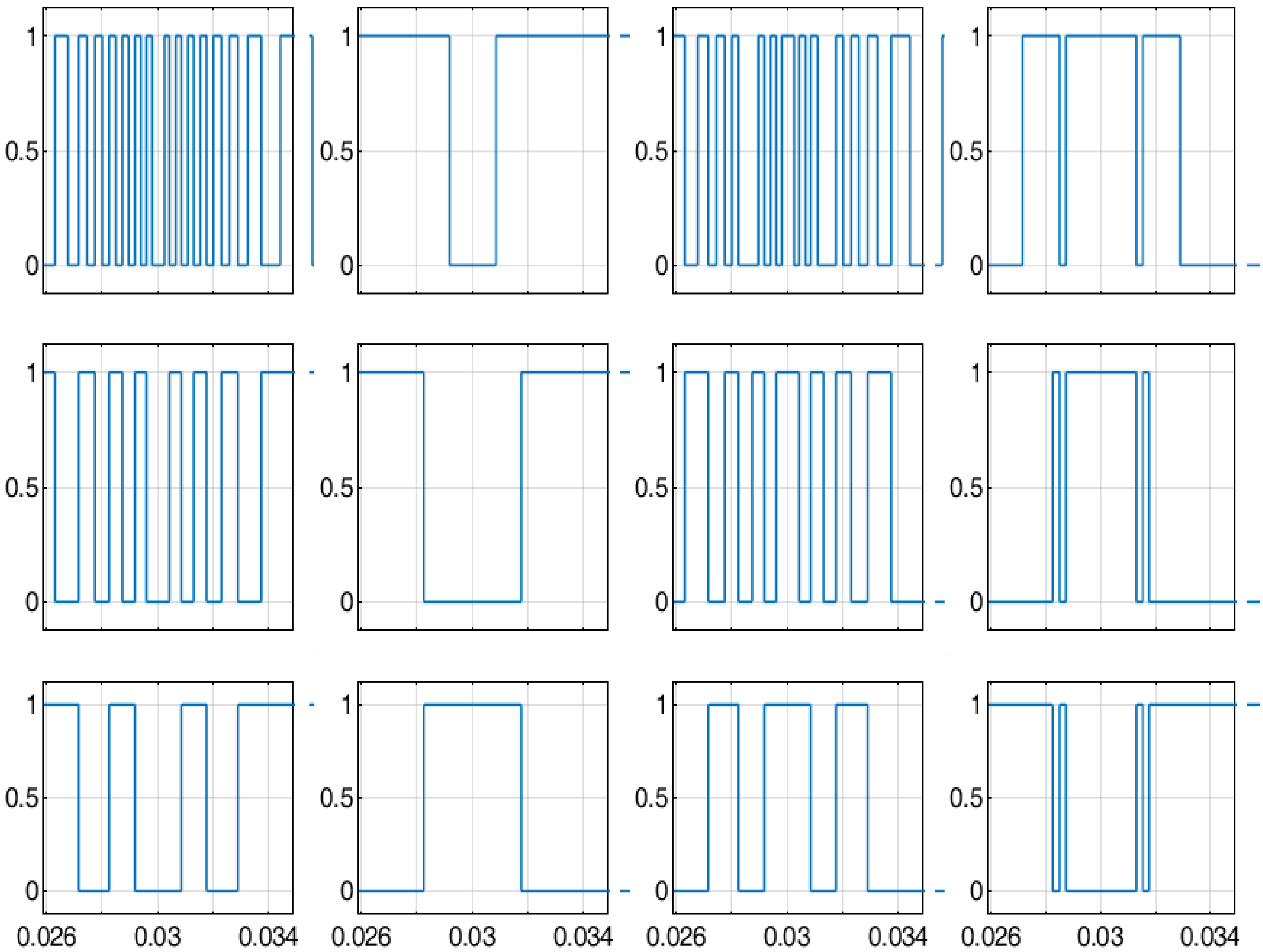

Figure 12. Gate Pulses to Inverter.

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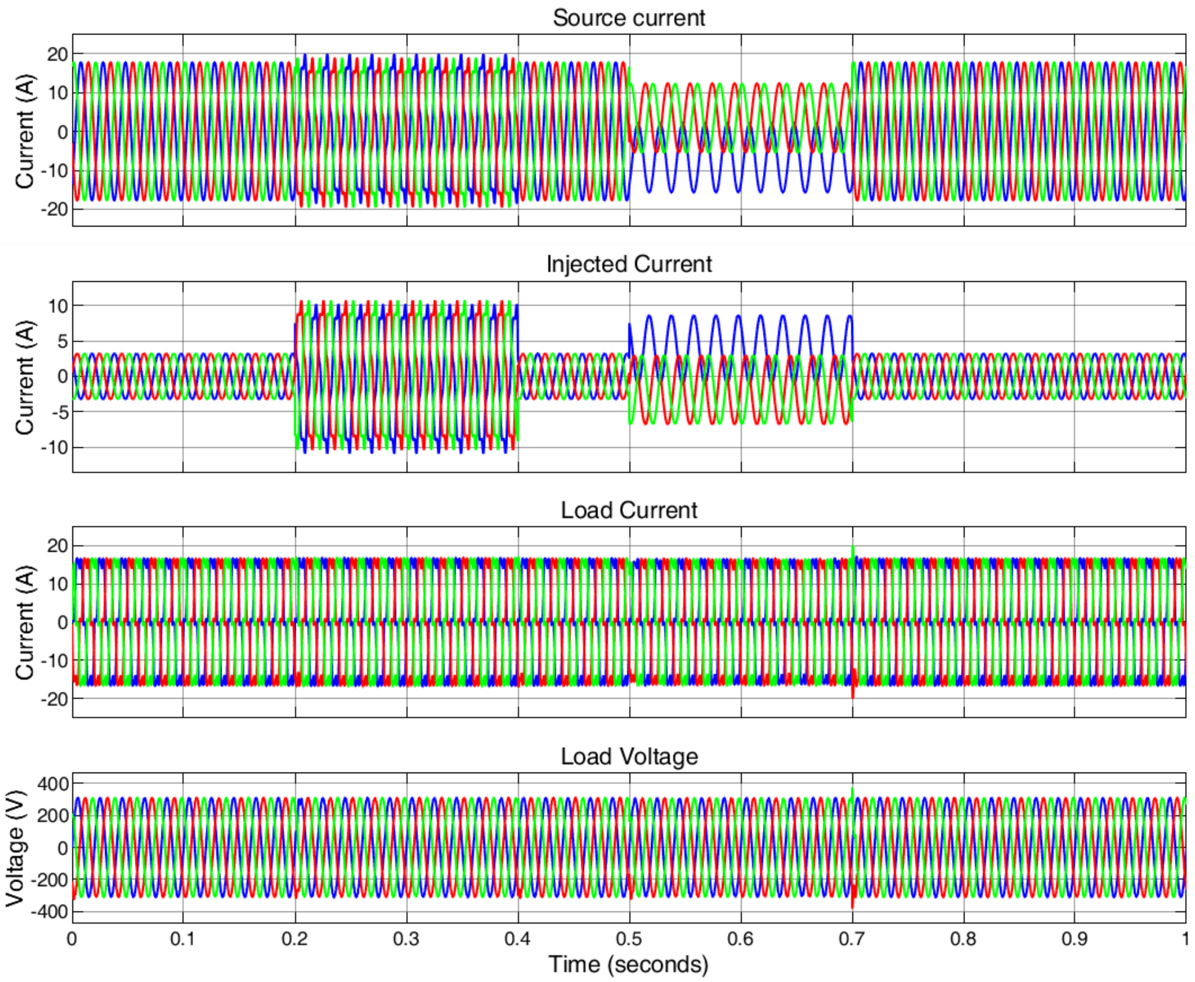

Figure 13. Source current, compensated current, load current and load Voltage.

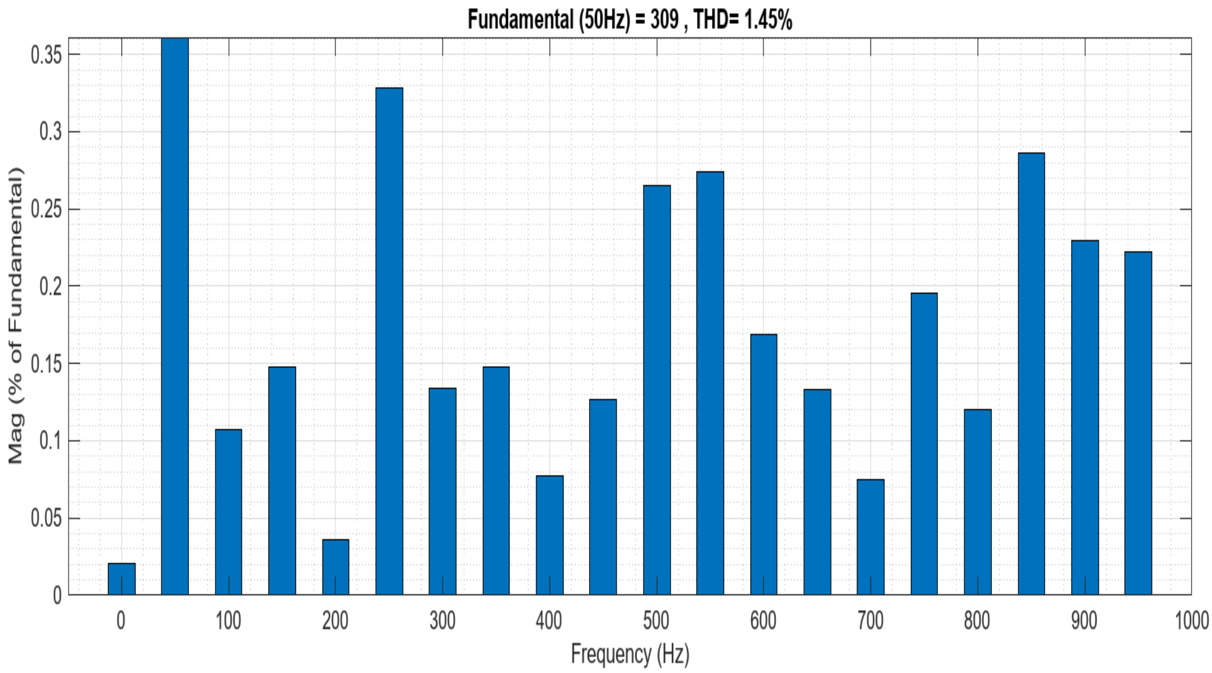

Figure 14. Harmonic analysis of proposed Dstatcom Model.

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For the proposed asymmetric multilevel inverter, the switching pulses are produced using the Coati optimization algorithm for 12 switches in the level generation part as shown in Figure 12. Figure 13 above illustrates the performance of the shunt compensation of Dstatcom under voltage sag and swell conditions, utilizing the Coati optimization algorithm. The simulation waveforms of the source current, compensated current, load current and load voltage are represented where compensation of swell is effectively done in 0.2ms to 0.4 ms and also compensation of sag is effectively done in 0.5ms to 0.7ms time period using asymmetrical multilevel dc link inverter as Dstatcom. Harmonic analysis confirmations that the compensation is done with 1.45% THD which is improved from 13.23% as shown in Figure 14.

Conclusion

This proposed research work introduces a DSTATCOM featuring an innovative 125-level asymmetry multilevel inverter structure. This structure offers the advantage of employing a flexible configuration, similar to traditional three-phase two-level voltage source inverters. The proposed 125-level asymmetry multilevel inverter is proposed for improving power quality and suppressing harmonics. Despite its minimal components, the inverter can generate 125-level voltages per phase. The total harmonic distortion (THD) of the output voltage remains below 1%. Each output voltage level of the AMLI is precise and stable due to the implementation of bi-directional DC-DC converters as the DC links of H-bridges, ensuring steady DC link voltages. These bi-directional DC-DC converters enable power transmission in both directions, thereby preventing a potential increase in DC link voltages. The Coati optimization algorithm determines the precise switching angles to produce gate pulses for the proposed inverter, achieving a 125-level output with low harmonic content and compensating for source current swell and sag in the grid.

Acknowledgement

We hereby declare that this submission is entirely my work, in my own words, and that all sources used in researching it are fully acknowledged and all quotations properly identified.

Conflict of Interest

The authors declare that there is no conflict of interest.

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