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A Dynamic Supply Modulator in 18 nm FinFET Node Using Comparator Approach

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Abstract: To keep up with the rapid development and to increase spectral efficiency, emerging communication systems like 5G will need to transfer data at speeds significantly faster than those of current systems. The subject of this study is radio frequency (RF) circuit systems, with an emphasis on efficiency enhancement for RF power amplifiers (PA). To cut costs and size, the majority of a smartphone's components are now integrated into a single chip. Regardless of the input signal's magnitude, the fundamental idea behind the envelope tracking (ET) approach is to operate the linear PA in its high-efficiency area. This is achieved by modulating the linear PA's supply voltage, which is as low as 1V, after determining the input signal's magnitude. In view of reducing the chip area and enhancing the efficiency of the PA, an 18nm FinFET node has been used and a comparator-based approach is demonstrated. Keeping the parameters of the 5G specifications in mind, a single-bit comparator is designed to operate at the Sub-6 GHz frequency band with a centre frequency of 3.5 GHz. The propagation delay of the comparator is as low as 67.18ps, and the 8-bit comparator, designed by cascading single-bit comparators, serves as the dynamic power source for the supply modulator. This study provides scope for further development in integrating the comparator with an RF PA for efficiency enhancement. The digital approach of using a comparator instead of bulky circuits provides an upper edge in terms of power consumption and reduction in chip area. The power consumption of the entire efficiency-enhanced PA in an 18nm FinFET technology is expected to reduce considerably in comparison with the CMOS technology.

Introduction

An electronic device's power, speed, and area are important factors, particularly in contemporary VLSI technology. In response to the rapid increase in data and video capabilities brought forth by fourth, fifth and advanced generation (4G, 5G) services, increasingly sophisticated signal modulation algorithms have been devised. The latest network standard, fifth-generation (5G), aims to outperform 4G networks by a factor of 100. 5G would offer better service quality, minimal latency and great data speed. An effective wireless access method that may increase wireless area throughput without using more bandwidth is required to meet mobile communication needs (Bhadada, 2023). Physical constraints are major in determining the high-level system requirements (Moraes et al., 2019). With the rise in popularity of portable electronics, power management has emerged as a key concern for producing small, light devices, especially in terms of extending battery life and maintaining acceptable performance. Its two primary power users are a portable system's processor and wireless communication transmitter (Cervera and Peretz, 2016). The frequency division of 5G advancements is divided into the sub-6 GHz band, also called frequency range 1 (FR1), and the 24 to 52 GHz band, sometimes called frequency range 2 (FR2) and 5G Plus. Designing

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the 5G new radio (NR) to deliver 5G services requires optimal utilization of available resources, including spectrum and technology. Exploring extra spectrum more efficiently for cellular communications has continued since the 1G period, and possible cellular bands at 3-6 GHz or above have recently received substantial attention (Huo et al., 2019). The Power Amplifier (PA) is a necessary component of a successful wireless communication system, and it is also the part of the radio frequency (RF) transmitter section that consumes the most power (Barmala, 2019; Sharan et al., 2024). Since conventional linear PAs operate at relatively low efficiency and the modulated signals in modern wireless communication systems have a high peak-to-average power ratio (PAPR), substantial power consumption is unavoidable. Several researchers have turned to Envelope Tracking (ET) and Envelope Elimination and Restoration (EER) approaches to address this issue. Supply modulators and switching PAs with modulated RF input signals are needed for ET, while supply modulators and switching PAs with a constant-envelope RF signal that only contains phase information are needed for EER. By adjusting the PA's supply voltage based on the output power level, internal power consumption is reduced at all power levels and the efficiency of amplifying a modulated signal is enhanced. Because of the broad requirements for intermediate frequencies, not all ET/EER PA variations are appropriate for 5G; consequently, supply-based adaptive bias and adaptive (multimode) implementation may be the most appealing options. The best options for low- and high-frequency 5G range mobile applications implemented in CMOS process are Doherty Power Amplifier (DPA) and variants of ET/EER PA, according to the review provided in the article (Vasjanov & Barzdenas, 2018).

Compared to EE&R techniques, ET offers greater supply waveform shape freedom since the RF output signal is amplified from the input signal (Leng et al., 2022). Consequently, envelope shaping is crucial in defining the relationship between the power supply and RF power by regulating ET efficiency and linearity. The supply modulator and RF PA design may be highly versatile in terms of efficiency, linearity, and bandwidth by utilizing shaped waveforms. (Wang, 2015) (Mariappan et al., 2022). Since the entire efficiency of the ET PA is determined by multiplying the supply modulator's and RF PA's efficiencies, an efficient and broadband supply modulator is an excellent indicator of overall efficiency in an ET PA. As a result, the supply modulator design is thought of as the main ET PA technique. The three new members of the linear modulator family are the power digital-to-analog converter (DAC), the class-AB/B amplifier, and the class-G/H amplifier. ETPA can use both analog and digital signal processors to apply envelope detection techniques. A range of architectural adjustments, such as switching, adaptive biasing, and linear biasing methods, are available to ETPA regulator designers. Precise synchronization between the regulator and PA is required. In order for the supply voltage to follow the envelope and achieve maximum efficiency, the RF path and the regulator need to be in phase. In addition, the utilization of switching regulators results in noise generation in the PA's supply rail and restricts its operational bandwidth. (Mariappan et al., 2020). A simple switch-mode power supply (SMPS), multilevel and multiphase converters, and other components are part of the discrete supply modulator family. Ultimately, these hybrid kinds can be classified as serial, parallel, or combination hybrids. Applications requiring large bandwidth, like data collection systems, radar processing, and communications, employ analog to digital converters, or ADCs. ADC development must meet several important criteria, including small chip size, high speed, low noise, low power supply operation, and low power consumption. Since comparators are essential components of ADCs, their performance is a determining factor in ADC performance. Nanoscale CMOS transistors with extremely low threshold voltages are needed to lower the operating voltage of dynamic comparators (Jain et al., 2021).

The envelope amplifier efficiency and RF power amplifier drain efficiency can be generally multiplied to find the total efficiency of the ET PA system, which is represented as

$$\eta_{overall} = \eta_{Envelope\ amp} * \eta_{RF\ PA} \quad (1)$$

In order to realize system-on-a-chip (SoC) and lower the cost and size of mobile devices, RF integrated circuits (RFICs) must be integrated with baseband processors. For the SoC, the RF PA is the most difficult component to incorporate. Due to reliability and performance difficulties, the RF PA is often based on a GaAs substrate, while most other chips are based on CMOS substrates. Compared to CMOS substrates, GaAs substrates are more expensive and have a lower integration capacity. Because of this, PAs will eventually be integrated into a silicon-on-insulator (SOI) process with switches or a CMOS substrate with RFICs in order to reduce chip area and subsequently the cost (Park et al., 2016). Different kinds of CMOS PAs have been effectively applied in contemporary wireless communication systems. A number of metrics were

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employed to assess the CMOS PAs' performance. Output power, power consumption, power gain, linearity, and power-added efficiency (PAE) are the key components of a PA design. It is impossible to avoid trade-offs between these variables, and these trade-offs complicate CMOS downscaling. The CMOS technique has become increasingly widespread because of its ease of use, low power consumption, and inexpensive design expenses. Nevertheless, the hot electron effect and oxide breakdown present problems for these PAs. The rationale is because power amplifiers run at high voltage, whereas CMOS technology is largely geared for low voltage. CMOS transistors' low breakdown voltages in PAs lead to a reliability issue (Arif et al., 2019). Microelectronic circuits are being scaled towards sub-10 nm technologies due to intensive research into minimising power consumption and improving device performance without compromising cost/function or yield performance. The design solutions by (Lin and Patterson, 2020) demonstrate how the various processes are suitable for operation in various 5G frequency bands. In the low frequency sub-6 GHz region, 0.25 µm GaN HEMTs are the optimum answer. However, 0.15 µm GaN HEMTs are recommended in the high frequency mm-wave band. To support the anticipated System-on-Chip (SoC) applications, advanced device architectures such as FinFETs, TFETs, Gate-All-Around (GAA), and horizontal and vertical nanowires (NWs) are needed for both logic and analog/RF building blocks (Claeys & Simoen, 2019). CMOS PAs are now a key barrier to achieving an ultra-low-cost single-chip RF system. Over the past ten years, significant advancements in circuit and design innovation have improved CMOS-based PAs' output power and efficiency. Simultaneously, a great deal of work is needed because new applications in the millimeter-wave bands and CMOS PA design become more challenging due to technological developments (Niknejad et al., 2012). One of the most difficult areas of study is reducing leakage power consumption, particularly in on-chip devices, which double every two years. It is more difficult to reduce static leakage power than dynamic leakage power because, in dynamic power, leakage power is determined by the number of transistors, their operational condition, and their type without consideration of switching activity. Subthreshold leakage current degrades devices' electrical properties and reduces their reliability (Kajal & Vijay Kumar Sharma, 2020). Nanoscale FinFETs may overcome electrostatic limitations, but parasitic components still play a significant role. The close proximity of the source/drain selective epitaxial growth (SEG) region to the gate increases fringe capacitances, while the narrow fin width increases series resistances. Parasites have been found to drastically reduce RF performance (Sohn et al., 2012). This work is focused on designing an 8-bit comparator circuit for envelope tracking that acts as an input to the supply modulator and will decide the amount of current required to amplify the incoming signal. Signals with low strength will require less current. The comparator-based ET will track the signal strength and the multilevel comparator circuit will turn on only the appropriate comparator outputs based on the signal strength. The supply modulator circuit that receives input from the multilevel comparator will turn on only those transistors that receive the appropriate signal, thus modulating the supply voltage received by the PA. This circuit is designed using 18nm FinFET PDK in the Cadence design suite. The purpose of this study is to validate the possibility of using lower node technology to replace CMOS and bulky circuits as an efficiency enhancement technique, thereby working at a supply voltage as low as 1V.

Proposed Method

The system design follows the flow diagram as shown in Figure 1.

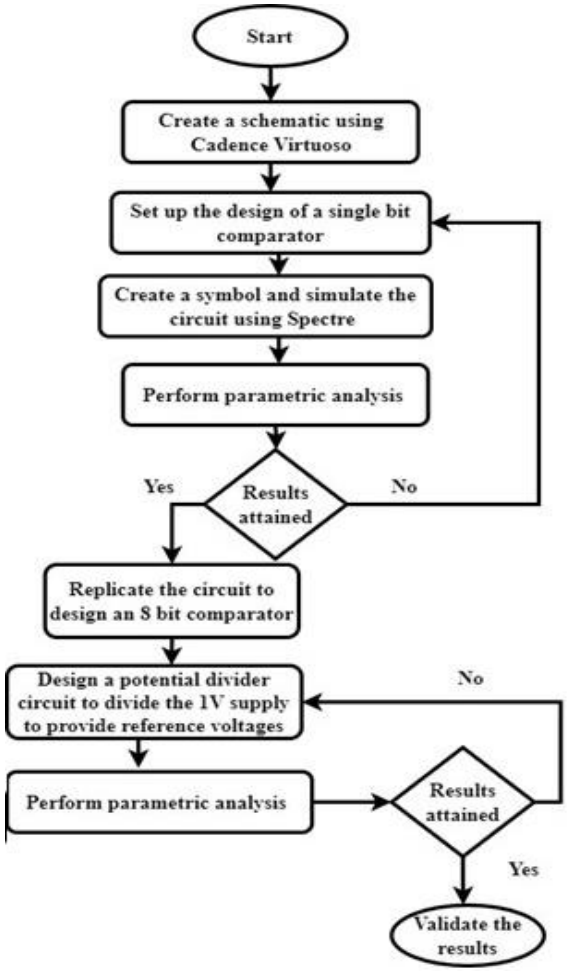

Figure 1. Flow diagram of the design process.

The circuit is designed using the instances in the library of the Cadence Virtuoso 18nm FinFET Generic Process Design Kit (GPDK). The instances are then placed according to the circuit and proper supply voltage and bias voltages are applied to the circuit. Parametric analysis is performed until the required results are obtained.

Single bit comparator

Signals that need to be converted from analog to digital require comparators. ADCs use high-speed, low-power comparators as fundamental, necessary parts. Current signal processing and transmission systems demand low power, low latency comparator. Comparators take two analog input values and provide a logical output value equal to the difference between the two input values. Static and dynamic are the two basic circuit design techniques that can be used to build comparators. Nevertheless, because they are always turned on, comparators with a static circuit design approach use much power. However, the use of a clock signal by dynamic comparators eliminates this static power usage. The comparator enhances reliability by considering the concept of redundancy in analog circuits. Single Upset Transients (SUT) is a type of transient error that can have a variety of effects on analog circuits, including total failure of the DC common mode voltage depending on the quantity of charge injected. Analog comparators, also referred to as analog checkers—have been the subject of in-depth research previously.

A series of inverter stages followed by latches is the foundation of most checkers. Error thresholds allow them to be divided into three categories: constant, relative, and adaptive. The size of the circuit directly affects how susceptible it is to transient faults and device degradations. Thus, we require a more straightforward comparator with fewer transistors in order to create an extremely dependable and fault-tolerant ADC. A comparator circuit with as few as 7 transistors is illustrated in Figure 2. This results in lower size while maintaining compatibility. Two inverters are used after the comparator output to produce the buffered and inverted output that the supply modulator circuit requires.

The comparator compares an input voltage (V_{in}) with a reference voltage (V_{ref}) in order to transform the Vin to logic '1' or '0'. V_{in} larger than V_{ref} causes the comparator circuit to saturate, which results in an output of '1'; otherwise, the output is '0'.

The gain of the comparator is given in equation 2.

$$\text{Gain} = \frac{V_{out}}{V_{in} - V_{ref}} \approx [\, g_{m22}(r_{022} \parallel r_{012})[g_{m4}(r_{04} \parallel r_{032})] \quad (2)$$

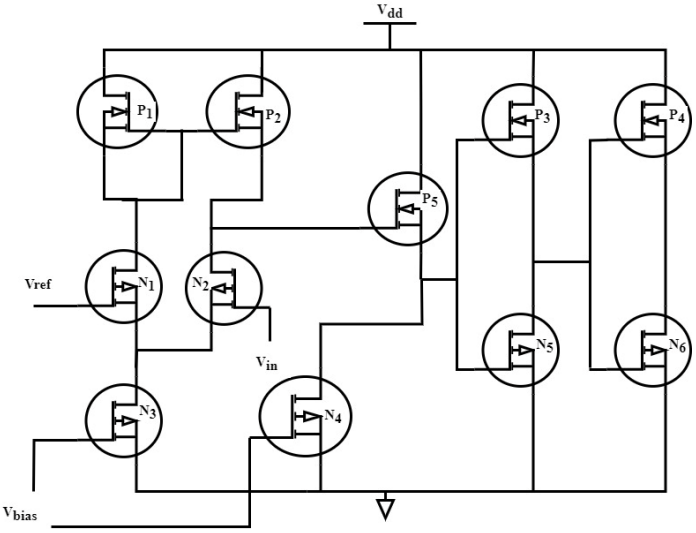

Figure 2. Single bit comparator.

where g_{mi} and r_{0i} are the transconductance and output resistance of the i[th] transistor, respectively.

$$\begin{cases} g_{mi} = \mu . C_{ox} . (W/L) \left(\frac{W}{L}\right)_i . (V_{gs} - V_{th}) \\ r_{0i} = \frac{2 . K_1 . L}{\mu . C_{ox} . (W/L)_i . (V_{gs} - V_{th})^2} \end{cases} \quad (3)$$

where W/L is the aspect ratio, μ is the mobility, C_{ox} is the capacitance of the oxide and $V_{gs} - V_{th}$ is the overdrive voltage of the transistor. For long-channel devices, the equations mentioned above are merely estimates and do not consider variables like channel length modulation and other second-order effects. As a result, the comparator's actual gain may differ slightly from its theoretical value in certain cases, even less. One of the key characteristics of our comparator is its high tolerance to variations in V_{thp}, V_{thn}, and T_{ox} resulting from aging, degradation, and temporary errors (Askari et al., 2011).

FinFET Vs CMOS

In the past ten years, a significant amount of research has been directed towards the optimization of numerous advanced process modules, including but not limited to stress engineering, ultra-shallow junctions, gate-stacks (high-l materials, cap layers, metal gates), silicides, raised source/drain for resistance control, contact technology, low-l dielectrics for multi-level metallization schemes, Cu interconnects, and so on. As we reduce the size of the device, numerous researchers point out the shortcomings of CMOS technology. The primary disadvantage of short channels is that they can cause leakage current during the off-state transition of bulk CMOS devices. Because of their lower transistor drive current, bulk CMOS devices do not fulfill industry criteria. In addition, gate oxide thickness must be taken into account when calculating the scaling factor. The gate oxide thickness has a fundamental limit that, when exceeded, results in an unanticipated gate leakage current. By creating high

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permittivity gate dielectrics, or "High-K," researchers hope to solve such issues. High driving current results from maintaining low sheet resistance. This leads to a steady transition in technology from bulk silicon CMOS devices to ultrathin body transistors. This ultrathin body transistor reduces subsurface leakage routes by creating thin silicon on insulator. Nevertheless, a thin body MOS transistor's parasitic drain and source resistance is extremely high. The least effective regulated gate is seen in ultrathin body MOS transistors. One of the biggest problems with ultrathin MOS devices is their thin bodies' high series resistance. Because of the FinFET's strong performances in the nano-dimensional range and ability to solve the short channel effect issues with traditional planar MOSFETs, many researchers have focused on it throughout the past 10 years. Researchers and the semiconductor companies are paying more attention to the FinFET results due to their exceptional short-channel behavior. Extrinsic capacitances of FinFETs become greater than intrinsic capacitances as the channel length decreases to less than 100 nm. This considerably decreases their RF performance since the extrinsic parasitic components outweigh the total gate capacitance. Reducing fin spacing, increasing the fin aspect ratio H_{fin}/W_{fin}, and a S/D fin extension can all lead to improvement. With today's technology, a 40nm-node FinFET may increase its highest attainable power gain cut-off frequencies by 80% and its current gain by around 40% through fin layout optimization and fin shape design with W_{fin} = 12nm, H_{fin} = 60nm, S_{fin} = 30nm and L_{ext} approximately 10nm (Tinoco et al., 2013). Using 7nm FinFET technology, a Schmitt trigger was examined for area requirements and frequency range by increasing the fin count and varying the supply voltage. According to the findings, adding more fins resulted in increased chip area and requires increasing width and height; additionally, lowering the supply voltage raises the working frequency to 5GHz. (Leonardo B Moraes et al., 2020). These results encourage RF circuit design in the analog domain.

8-bit Comparator

Figure 3 illustrates how eight single-bit comparator circuits are cascaded together to form the 8-bit comparator circuit. The comparator receives its input from the envelope detector's (V_{env}) output. The reference voltage for each of the eight comparator circuits is gradually varied from 0 to 1 V using a potential divider

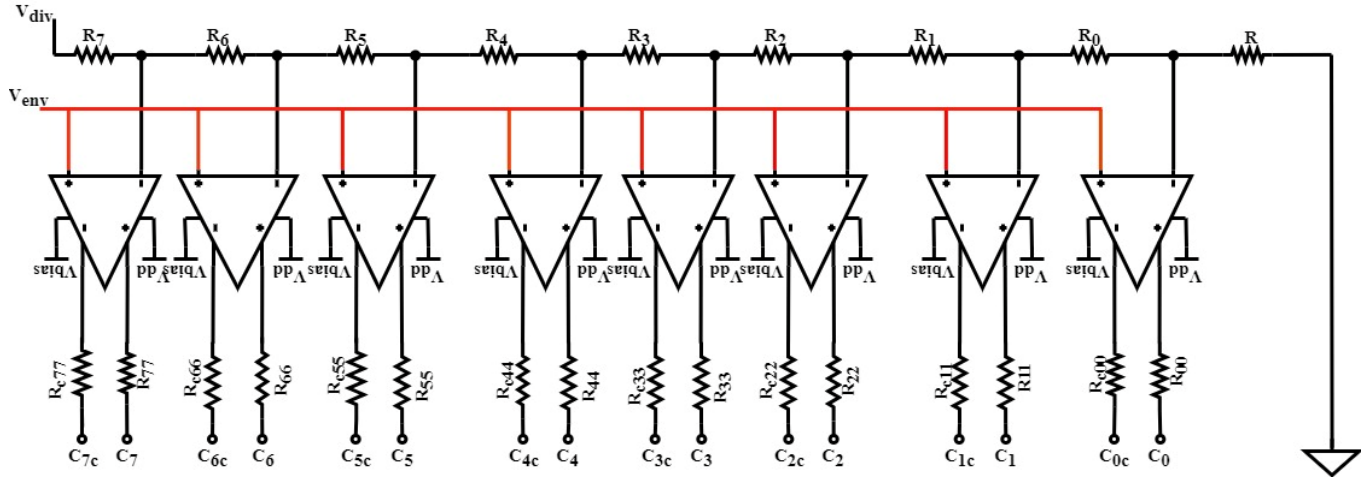

Figure 3. 8-bit comparators cascaded and potential divider for Vref.

circuit that has been designed to divide the reference voltage proportionately among them. A potential divider circuit has been constructed to divide the reference voltage evenly among the eight comparator circuits and progressively vary each comparator circuit's reference voltage from 0 to 1V. Each comparator block's reference voltage will be compared to the input, which is the envelope detector circuit's output signal. The comparator will turn on every comparator output where the reference signal is larger than or equal to the voltage of the envelope signal. Thus, it is expected that if the signal strength is low only the corresponding number of comparators will turn on and the rest of the comparators will remain off. A supply voltage, V_{dd} of 1V is applied.

Results and Discussion

Practical Set-up

The 18nm FinFET Generic Process Design Kit (GPDK) has been extracted into Cadence Virtuoso simulation tool to obtain the library. From the various transistors available in the library, due to results reported by (Jaisawal et al., 2022), for analog/RF high voltage threshold (HVT) performance deteriorates in comparison to low voltage threshold (LVT), here LVT is preferred for both PMOS and NMOS. In order to gain insight into analog/RF applications and linearity performances, the suggested study offers a comprehensive design guideline for the appropriate FinFET architecture. Table 1 provides

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the values for the optimised device available in the 18nm FinFET GPDK of Cadence that provides the required results.

Table 1. Device sizes.

Device	Fins	Fingers	Multiplier
L = 18nm			
P_1, P_2, P_3, P_4	2	1	1
P_5	2	1	4
N_1, N_2, N_3, N_4, N_5, N_6	2	1	2

voltage and input voltage, which is actually the envelope signal. For this, the FinFET is optimized by adjusting the number of fins (n_{fin}) and fingers (n_f) of the PMOS and NMOS transistors. In the circuit the n_{fin} = n_f = 2 for NMOS and n_{fin} = 2 and n_f = 1 for PMOS. The comparator is tested by carrying out parametric analysis for various values of V_{bias} from 100mV to 1V and V_{dd} = 1V. Since we aim to design the comparator with high switching speed and the least delay, for the 5G communication in the Sub-6 GHz frequency range, a 3.5GHz frequency input signal is applied. The FinFET-based comparator circuit is

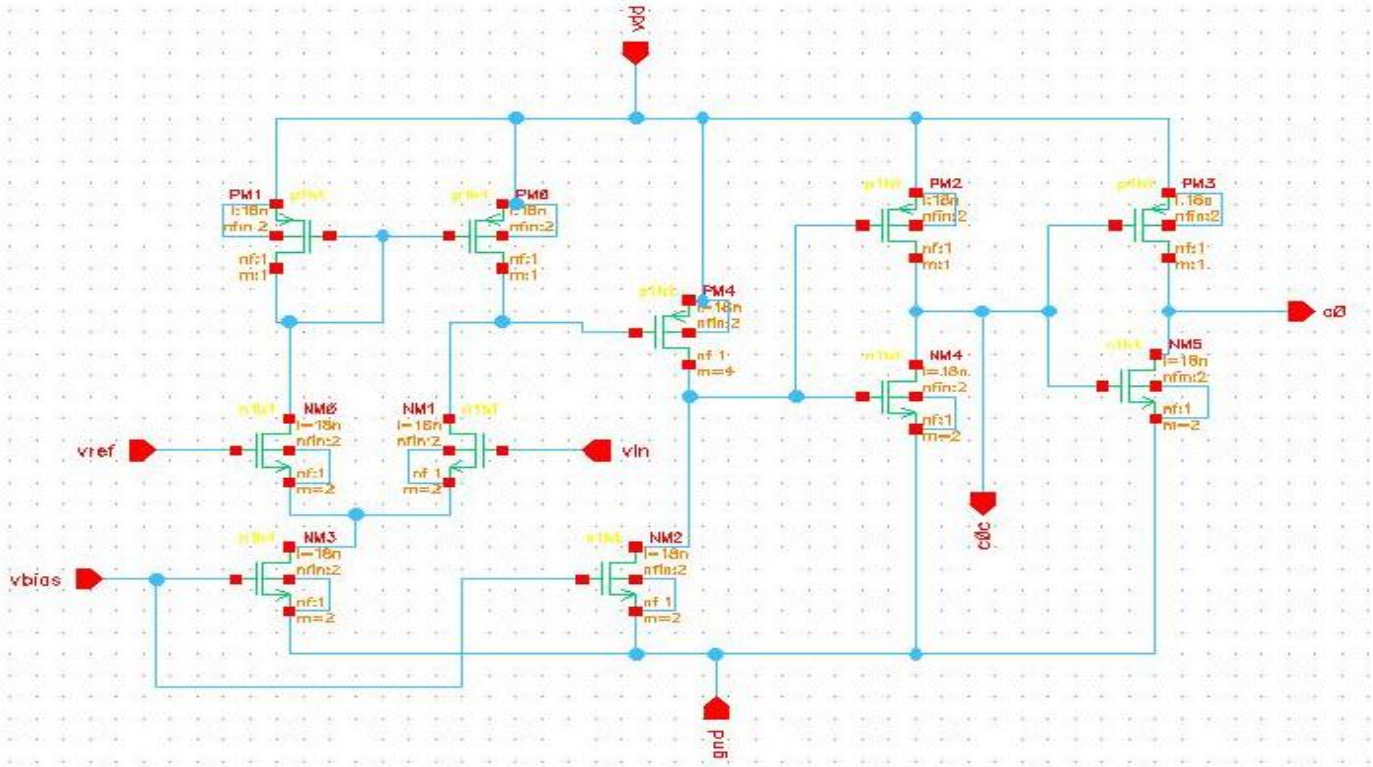

Figure 4. Practical Set-up for single-bit comparator (extracted from Cadence tool).

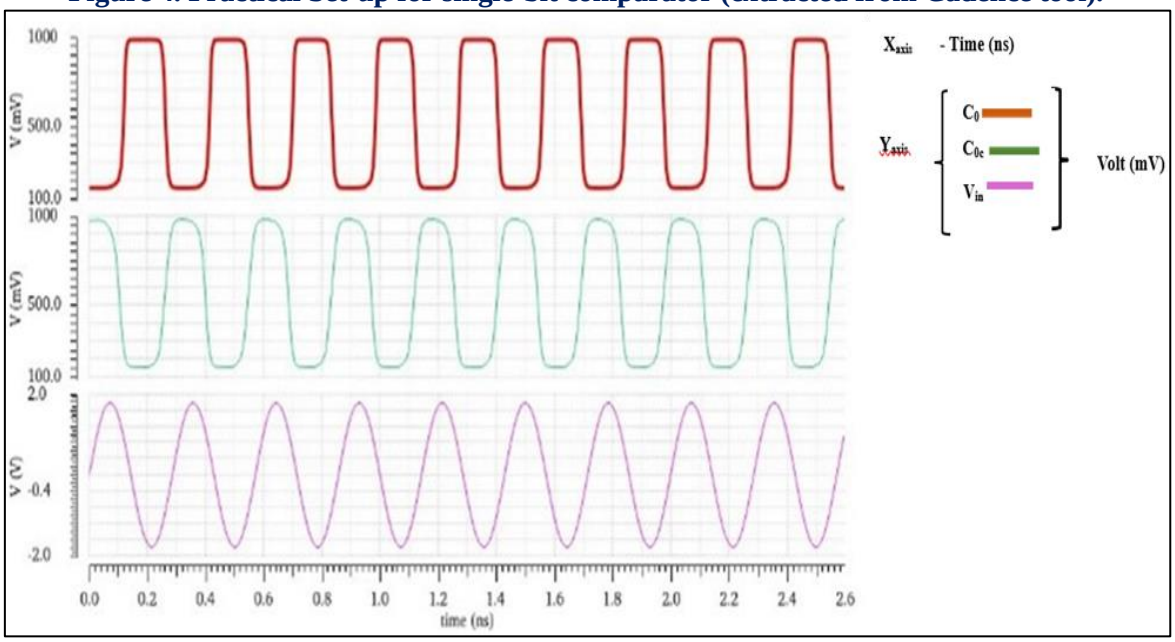

Figure 5. Single bit comparator output (extracted from Cadence Spectre tool).

It is important to optimize the FinFET for operation as a switch that turns ON and OFF based on the reference shown in Figure 4, and the results obtained at Vbias = 0.3V are shown in Figure 5.

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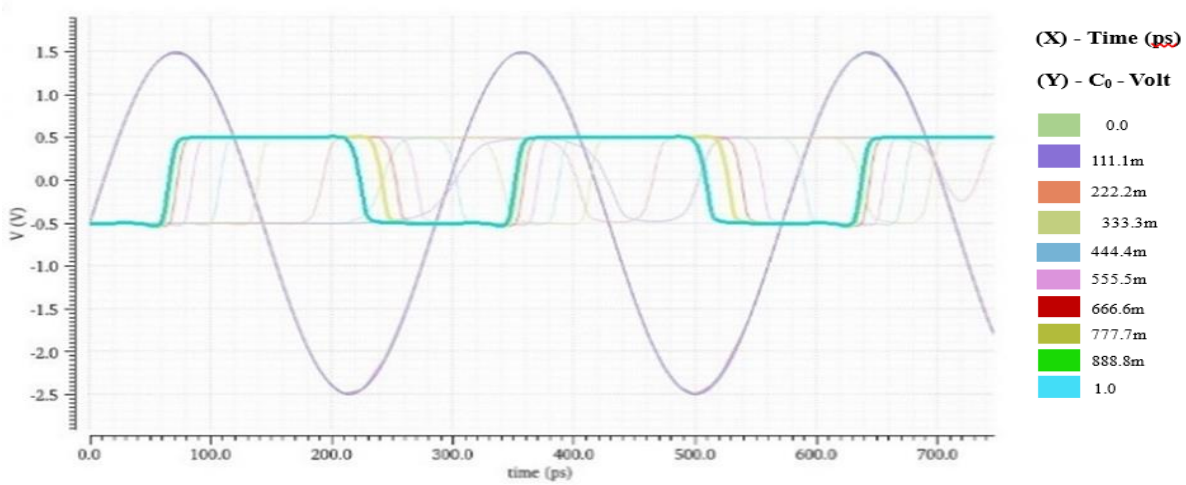

Figure 6 Propagation delay for V_{ref} from 0 - 1 V (extracted from Cadence Spectre tool).

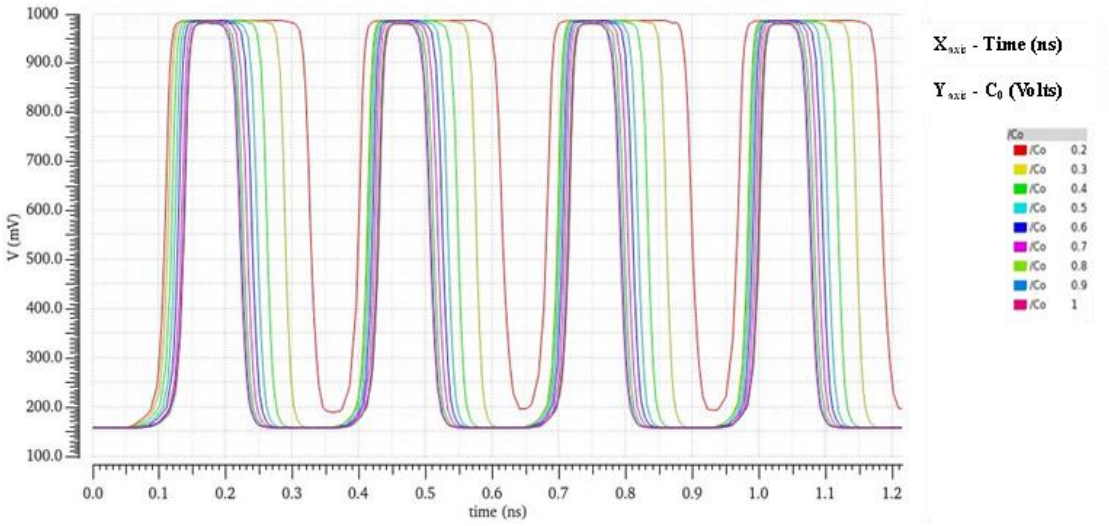

Figure 7. Comparator results for various values of V_{ref} obtained by parametric analysis.

Single-bit comparator results

The comparator result in Figure 6 shows that the propagation delay is approximately 5ps which is much below the one using CMOS fabrication method as in (Fouzy et al., 2017) (Shah et al., 2022) and the 18nm FinFET technology as in (Vallabhuni et al., 2020). Reference voltages between 0.2 volts and 1 volt were used to validate the comparator. Analysis revealed that the propagation delay was significantly larger at lower reference voltage values and decreased at higher V_{ref} values.

Using a range of V_{ref} values, the waveform in Figure 7 shows how a single-bit comparator operates. For this reason, we consider V_{ref} to be 1 V. The computed average of the rising time delays (tpdr) and fall time delays (tpdf), respectively was 67.49 ps. When numerous single-bit comparators are cascaded together, they can be configured to turn on or off in response to the reference voltage, as shown by the parametric analysis for different reference voltages in Figure 6.

Table 2. shows a comparative analysis of the comparators designed using various technologies and the propagation delays obtained for the operating frequency.

Table 2. Comparison with previous work using different technology nodes.

Reference	Technology	No. of Transistors	Propagation delay (s)	Frequency (Hz)
(Kawatra & Bhatia, 2018)	90nm CMOS	-	0.15n	6.7G
(Kundu et al., 2018)	30nm FinFET	-	9.2n	108M
(Yu et al., 2020)	180nm CMOS	-	0.53n	50M
(Casañas et al., 2022)	180nm CMOS	10	7.5n	50M
This work	18nm FinFET	7	0.064n	3.5G

8-bit comparator results

Now, 8 such single-bit comparators are cascaded and the potential divider circuit dictates the Vref for each comparator. The Potential divider circuit is designed in

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such a way that the applied Voltage V_{div} is equally divided among the 8 individual comparators. The potential divider circuit comprises of 8 resistors of 10Ω. This potential divider circuit obtains the 8 reference voltages for the 8 comparators. It is possible to adjust the required voltage levels by designing appropriate values of the potential divider resistors accordingly. Assuming the power amplifier designed in (Gangadharan et al., 2024b) using the 18nm FinFET technology where the input power of the range from -20dBm to 2dBm is amplified to 6dBm with a maximum gain of 27.71 dB and the output voltage being 1V. If the same circuit is used as a pre-amplifier and the output passes through an envelope detector circuit that ceils the signal to 1V, then the designed 8-bit comparator is good. Figure 8 represents the output of the 8-bit comparator obtained by cascading 8 single-bit comparators provided with appropriate potential dividers for various voltage levels. This indicates that the appropriate number of comparators will be turned on based on the signal strength.

receive the signal from a single-bit comparator, as shown in Figure 9. N_0 and N_{15}, two NMOS transistors, work as a pair and receive inputs that complement each other from the circuit, C_{0c} and C_0, respectively. Therefore, when one transistor is ON, the other transistor is OFF due to the complemented input on the gate of the transistor. Now, depending on the outputs from the complemented and uncomplemented outputs from the individual comparators of the 8-bit comparator shown in Figure 8, corresponding transistors turn ON.

The incremental increase in the number of transistors in the ON state results in incremental current at the node, according to Kirchoff's current law. This modulates the supply to the PA, which is connected to the output of the supply modulator. The output of the supply modulator is connected to the PA through a filter circuit, which also acts as a load. It also acts as the input impedance to the PA. This is the proposed circuit for the supply modulator, which is expected to control the input dc supply with respect to the biasing requirements in accordance with the

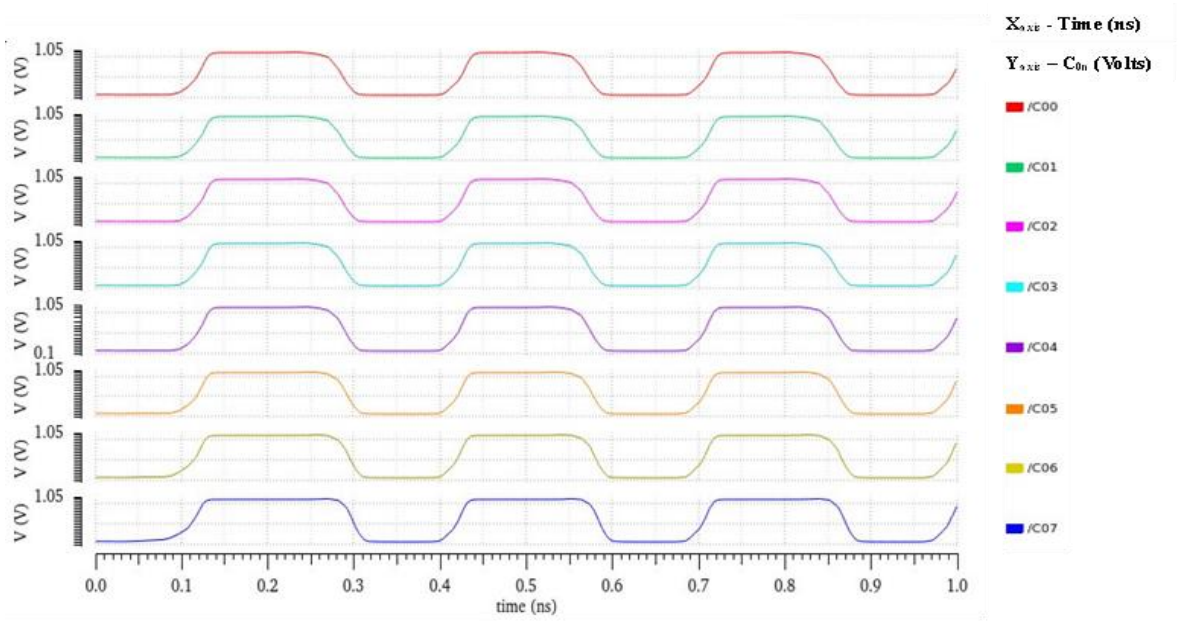

Figure 8. 8-bit comparator output.

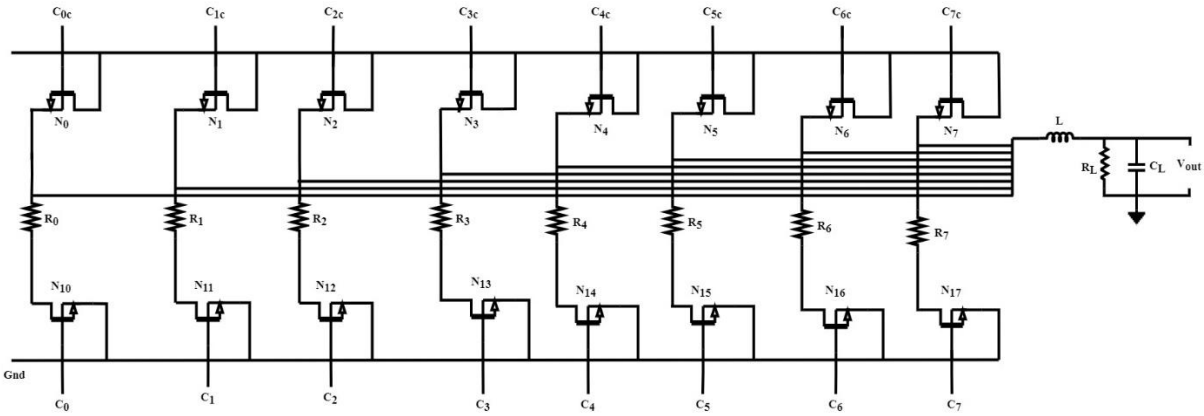

Figure.9. Supply modulator circuit.

The supply modulator that will be designed will comprise an array of 8 transistors that will individually input signal strength. The results of (Gangadharan et al., 2024a) using 130nm CMOS technology show that the

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supply modulator designed this way produces expected results.

Conclusion

A single-bit comparator has been designed using 18 nm FinFET node with as low as 7 transistors, excluding the buffer and complement stages. Taking into account the relative sizes of a CMOS and FinFET structure, as well as the power requirements in both cases, it is evident that the chip size is being reduced, which is further aided by the smaller number of transistors employed in this structure. The bias requirements and supply voltage are around 0.3V and 1V, respectively. The cascaded comparator circuit can operate effectively using the same biasing and supply voltage levels. The 8-bit comparator circuit has generated encouraging results in terms of processing speed in the picosecond range. This provides scope for designing an envelope tracking circuit at a higher speed and a PA fabricated on the same 18nm FinFET technology node. Future work will focus on lowering chip size by implementing all circuits, including the PA, on the same node and verifying the efficiency of the ET circuit.

Conflict of Interest

Authors declare no conflict of interest.

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