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A Study of RF Power Amplifiers for 5G and Future Generation Mobile Communication: Can FinFET Replace CMOS?

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Abstract: A low-power strategy that can manage analogue, digital, and RF functionalities on a similar chip is crucial for wireless systems. Various difficulties restrict the widespread adoption of CMOS power amplifiers despite the fact that they provide highly integrated, low-cost wireless communication. Some of the main issues with CMOS power amplifiers include non-linearity, low breakdown voltage, a lack of high-voltage capacitors, and incorrect RF models. The RF signal is amplified without distortions using a linear power amplifier (LPA), which is less effective whenever driven by constant voltage. In order to significantly enhance the effectiveness of the power amplifiers, three frequently utilised techniques—Doherty, envelope elimination and restoration (EER), and envelope tracking (ET) techniques are reviewed in this work. Results point towards ET approach as the one that is ideally suited for future mobile communication systems. The essential component of ET systems, the envelope tracking power source, is what determines how effectively the system functions. It also lists the benefits of FinFET technology over CMOS and looks at three well-liked techniques for increasing power amplifier efficiency. Considering the advent of mobile communications systems, the frequency band and peak-to-average power ratio (PAPR) are quickly growing, posing significant design issues. FinFET as an alternative may considerably reduce the chip area.

Introduction

The last operational element in contemporary radar and communication equipment's radio frequency (RF) chain is typically a power amplifier, sometimes referred to as a PA. Its nonlinear nature significantly influences system performance overall and is typically the element that turns out to be the biggest bottleneck in modern radio systems. The main purpose of a power amplifier is to increase a radio signal's strength to levels of output power required for wireless or wired transmission from a receiver to a transmitter (Nikandish et al., 2020; Gangadharan et al., 2024). This can be accomplished in a couple of different ways. They typically operate at rather high-power levels, and as a result, they account for a significant portion of the total power consumption in the transmitter system. On the other hand, the efficiency with which they convert the DC source power into RF output power is generally quite low. In addition, It is extremely reliant on the strength of the RF signal drive, and it peaks when the amplifier is used in the nonlinear part of its spectrum and the output RF power is compressed or perhaps saturated. For power amplifiers, efficiency and linearity are essential criteria, yet they are diametrically opposed to one another and are the most significant factors to be compromised (Pang et al., 2020; Varshney et al., 2024).

A low-power strategy that permits electronic, physical, and RF functionalities on the identical device is necessary for wireless applications. Maintaining leakage current

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levels that are regarded as acceptable becomes more challenging when CMOS is scaled beyond the 65 nm node. Because of this, we are actively investigating innovative materials and architectural designs, such as multiple gate transistors (e.g., FinFET). A FinFET's gate surrounds a thin "fin," which is a slice of silicon that is ideally undoped and runs along the top and side surfaces. The consequences of the short channel are reduced since the gate wraps across the channel. Scaled planar MOSFETs exhibit significant leakage, subpar matching, & noise deterioration, making it difficult to design analogue and RF circuits with them (Badal et al., 2019; Paul et al., 2023).

Therefore, based on experimental characterization, the current study examines the possibility of operating RF power amplifiers using FinFET technology over CMOS technology for analogue and RF applications. This review is based on the findings of the previous work. In this work, we talk about the CMOS Amplifiers, the design of low power RF Power amplifiers and linear power amplifiers, and the different classes of RF amplifiers. We will also discuss the efficiency enhancement methods for power amplifiers. This is followed by a discussion of FinFET's V-I characteristics and why they're advantageous over CMOS in RF amplifiers. Then, we go on to discuss the challenges and future perspectives of the RF Amplifier.

CMOS Amplifier

According to the advantages complementary metal-oxide semiconductor (CMOS) technology offers over GaAs (gallium arsenide) and GaN (gallium nitride) technologies, wireless systems for communication are currently increasing quickly (Waykole and Bendre, 2018). Due to the chip's small size, operating with a reduced power supply is possible thanks to CMOS technologies, reducing power dissipation in the circuit and lowering the cost of manufacture. RF, digital and analogue activities may all be integrated at a minimal cost using CMOS technology. The CMOS power amplifier (PA) might replace current wireless technologies to placate low-power and cost construction requirements.

CMOS PA has been extensively employed in various wireless communication applications throughout the years, including home automation, RFID, TV broadcasts, phones, and industrial consumer electronics medical equipment (Badal et al., 2019). Because ultrasonic imaging demands a better contrast resolution, which a very linear PA can achieve, It has been used to magnify high-voltage excitation signals and trigger ultrasonic transducers in high-frequency healthcare uses. They are also utilized in tablets, smartphones, and feature phones (Waykole and Bendre, 2018; Koo et al., 2012).

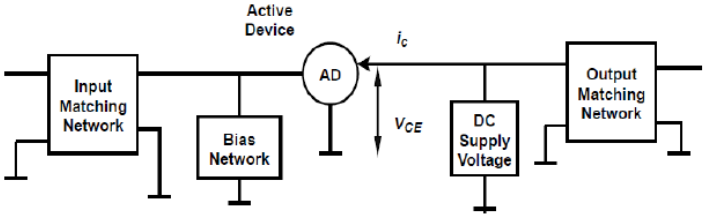

Figure 1. Block diagram of CMOS power amplifier is adopted from Band et al. (2019).

After completion of CMOS and its implementation, as well as the block diagram. Now we have briefed you about reviewing the performance parameters of a CMOS power amplifier.

Performance Parameters of CMOS

CMOS PA performance was assessed using a variety of factors. Linearity, power consumption, power added efficiency (PAE), Output power, and power gain are the most significant features of a PA design. These variables always result in trade-offs, which make PA design difficult at CMOS economizing. The following are the major elements for evaluating transmitter performance:

Output Power

Output power (Pout) is the most crucial part of a PA design (Fritzin and Alvandpour, 2010). Power gain and efficiency affect output power. Since heat drains power, the device's energy supply must exceed the needed output power (An, 2009). Current determines output power when the source voltage is constant. PA performance depends on output power, which is proportional to efficiency. Equation (1) gives dBm:

$$P_{out} = \frac{V_{out^2}}{2RL} \quad (1)$$

where RL is the resistance load, and V_{out} is the output voltage.

PA performance includes power usage. The growing need for portable operation must be met to maximize device runtime without wasting power. As indicated in Equation, a PA's total power consumption (P_{Total}) equals its dynamic and static power consumption. Leakage current (ICC) causes PS, whereas high-frequency switching causes PD.

$$P_{Total} = P_S + P_D \quad (2)$$

$$P_S = V_{DD} + I_{CC} \quad (3)$$

$$P_D = \left[\left(C_{pd} \times f_1 \times N_{SW}\right) + \sum\left(C_{Ln} \times f_{On}\right)\right] \times V_{DD^2} \quad (4)$$

Power Gain

Equation (5) defines power gain (G) as the input-to-output power ratio. This value indicates how well the power amplifier can provide a signal to the load that is

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substantially more powerful than the input power (Fritzin and Alvandpour, 2010). The gain describes how much a signal's amplitude has increased. A power amplifier boosts the output power to provide better sensitivity and efficiency (An, 2009).

$$G = 10\log_{10}\left(P_{out}/P_{in}\right)[dB] \quad (5)$$

whereas, P_{in} represents the input power and P_{out} the output power.

Efficiency

Two categories of the PA's efficiency—drain efficiency (DE) and power-added efficiency—can be made (PAE). According to Equation (6) (An, 2009), DE is the RF output power to DC dissipation ratio. According to Equation (7) (Fritzin and Alvandpour, 2010), PAE is calculated as the output power acquired minus the input power divided by the DC power dissipation. When the input power is considered, PAE measures how well the PA transforms the DC power into an AC power signal (Long, 2000). High PAE results from high output power.

$$DE = P_{out} / P_{(DC,drain)} \quad (6)$$

$$PAE = \left(P_{out} - P_{in}\right) / P_{(DC,drain)} \quad (7)$$

Linearity

Linearity occurs when the device output changes linearly with the input (Choi et al., 2015). RF communication architectures now value linearity. Linearity depends on the third-order intercept point (IP3). Plotting the output power vs input power graph on a logarithmic scale yields the intercept point (Choi et al., 2015). High linearity implies output power is proportional to input power (An, 2009).

Hence, PAs should have low power consumption, high output power, power gain, PAE, and linearity to meet demand. Power amplifier efficiency depends on PA and PAE output power.

Design of low-power RF amplifier

STI (shallow trench isolation) achieves electrical isolation between the devices, which is proceeded by low dose, high energy deep well implants. The gate oxide's equivalent oxide thickness (EOT) is 1.4 nm. A thin metal layer (5–10 nm) is placed for work function engineering, followed by a 100–nm polysilicon layer. In this instance, resist and hard-mask trimming along with 193-nm DUV lithography are used to define the gates. After the gate etches, shallow extensions (SEs) are prepared, and in addition to lessening short-channel effects, halos are then transplanted to improve local channel loading in the expanding region. To prevent the spread of the SE and halo implant, separators are initially constructed all around the gate before installing the deep source/drain (S/D) augmentations. The dopants are activated and implantation damage is eliminated by a single spike anneal. The S/D active and poly regions are siliconized to reduce contact and sheet resistance (Wang et al., 2020).

Power Added Efficiency and Linearity

Instead of "efficiency," many individuals prefer to use "power added efficiency" (PAE). The latter simply refers to the proportion of the input RF power to DC power pulled from the supply, which is not regarded as a clear measure or metric of the performance of the power amplifier. The former refers to or includes the input RF power. Power amplifiers should have great linearity and high power-added efficiency. Unfortunately, their relationship is inverse. Non-linear amplifiers can be utilized for constant envelope applications that utilize frequency-modulated signals (like FM and FSK). Additionally, linear amplifiers can be utilized for applications that use variable envelopes and amplitude-modulated signals (such AM, ASK, etc.). Depending on the application, a trade-off between efficiency and linearity may occasionally be necessary.

There are two main categories of power amplifiers, linear and non-linear. This criterion was selected because there are only two fundamental kinds of modulation: those with a variable envelope (also called amplitude modulation) and those with a fixed envelope (Frequency Modulation). The 7 signal's amplitude is quite important for AM systems because it carries the information. The usage of linear power amplifiers in AM systems is due to this. However, the amplitude does not carry the information with FM systems or constant envelope systems, which is why non-linear PAs are utilized with FM systems (Goswami et al., 2019).

Linear Amplifiers

The traditional topologies A, B, AB, and C are available for the group of linear power amplifiers. As already established, this set of amplifiers has the ability to amplify signals with irregular envelopes or signals with variable amplitude. All of these classes have the same topology, making it possible to build them all using the circuit. Bias conditions are the only thing that sets the amplifier class of operation apart. An approximately sinusoidal waveform powers all of these classes, and during at least a portion of the RF cycles, the transistors act as a regulated current source (Lazarevic et al., 2019).

Although it is not part of the basic schematic circuit for these amplifiers, it is advisable to use the tuned parallel LC filter, shown in Figure 2, to classify the signal outside the fundamental frequency. Considering that the load is only "seen" by the device at the fundamental frequency and functions as a short-circuit at all other frequencies, this

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tailored filter increases the amplifier's efficiency (Saed and Khaleel, 2022).

RF Power Amplifier in low-power CMOS

The technique known as silicon CMOS has quickly become the standard for integrated circuits. In the 1970s, CMOS gate lengths were 10 um, but today, they are less than 90 nm. This is a significant decrease in gate length. The International Technology Roadmap for Semiconductors (ITRS) published in 2004 predicts that by the year 2006, MOS transistors with a physical gate length of 80 nanometers will be readily available to the general public(Vasjanov & Barzdenas, 2018). Because of its scalability, it consumes less power while maintaining or even improving its performance levels. When CMOS devices are lowered down to dimensions of sub-100 nm, the deep sub-micron CMOS opens up new possibilities in the design of low voltage and current circuits (Zahid et al., 2021).

Low Supply Voltage Technique

For more than three decades, conventional CMOS technology has been confined to designing methods with high-performance digital circuits as the primary focus. The majority of the time, analog and RF designers stick to discrete solutions or hybrid blocks of bipolar GaAs, and more recently, they have been turning to BiCMOS and Heterojunction Bipolar Transistors (HBT) (Tochou et al., 2022). Not only are digital device models insufficient for realistic circuit simulation, but the design space available to analog/RF designers is also rapidly decreasing. This presents a significant challenge. The continuously falling supply voltage for current CMOS processes is one of the most challenging issues. This results in decreased voltage headroom and dynamic range for analog and RF applications (Manickam, 2019).

Challenges for Low Power Supply

Analog circuit power consumption is not necessarily reduced by reducing supply voltage as well as processing feature size; in actuality, this is typically the case. Electricity is used to keep the transmitted signal just above thermal noise level to obtain the optimum signal-to-noise ratio or dynamic range in analog devices. Power-efficient analogue circuitry should be built to optimize the voltage swing since the proportion between voltage levels and the ability to detect is related to the lowest power usage. In an attempt to reduce the supply voltage while maintaining the frequency as well as signal-to-noise ratio, its trans conductance should be increased. Usually, this is accomplished by sacrificing power or shortening the channel. Because of this, analog designs require a distinct approach (Saritha et al., 2019).

Fabrication Methods

In many ways, FinFET is different from planar bulk CMOS. FinFETs' three-dimensional architecture makes processing more complex and presents new integration difficulties.

FinFET devices are produced on SOI wafers through a p-type background depletion of around 15 centimeters. Due to a shortage of channels and extremely poor implantation, the fins are still incomplete. An anneal in an ambiance restores the side walls and softens the top edge after active area demarcation. In this study, two distinct gate stacks for FinFET transistors are taken into account. In one instance, a gate insulator with an EOT (effective oxide thickness) of only 1.9 nm is employed using a high-k gate metal gate stack. This gate dielectric was created by layering an interfacial oxide. A thin (5–10 nm) TiN metal layer is deposited on top of a 100–nm polysilicon layer to form the gate. The alternative flavour has a polysilicon gate and an EOT gate oxide in a more conventional gate stack featuring a 1.8-nm pitch. Employing 193-nm DUV lithography and painstaking mask cutting, the new work can produce gates as short as 45 nm. This phase of the lithography process is more difficult than it is for planar gadgets due to the steep topography of the fins. The gate's wrap-around form makes it easier to control short-channel effects, and halo implants could be avoided. After implanting shallow extensions, a spacer is created near the gate (Bruch et al., 2019).

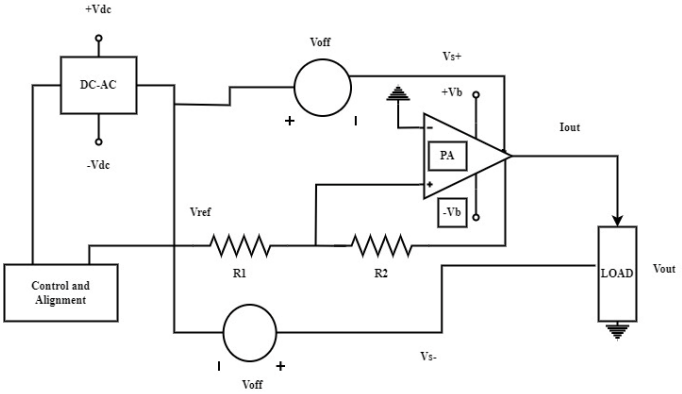

Figure 2. Linear power amplifier schematic is adopted from Lazarevic et al. (2019).

The operation class of linear amplifiers can be quickly determined by looking at the drain current waveform. The power amplifier operation class is determined by how much of the RF cycle the transistor is conducting (Saed and Khaleel, 2022).

The audio amplifiers most often used are A, B, AB, and C. Other Classes are contemporary amplifiers that drive the output load using switching topologies and PWM technology (Bortoni et al., 2002). In order to distinguish them as a new class of amplifiers, upgraded versions of

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conventional classes are sometimes given a letter designation. For instance, a customized Class B or Class AB amplifier is a Class G amplifier.

Table 1. Outlines both the advantages and the challenges of output phasing of Doherty architecture.

Advantages	Challenges
Can provide an extremely high level of efficiency compared to Doherty because both PAs in the out-phasing approach work in saturation.	Matching that is optimized and required for each path
	Branch loading is required when using out phasing over very broad dynamic ranges.

The drain efficiency of the various linear amplifiers is shown in figure 3. As previously mentioned, the class-AB and class-C amplifiers have a range of potential values that depend on the conduction angle (Choi, 2019).

Efficiency enhancement techniques for power amplifier

A PA is made to function properly at a certain input power. As input power is reduced, the PA's efficiency rapidly diminishes. A 3-dB decrease in input power causes a 3-dB decrease in output power for class B, but a 20% decrease in efficiency. Similarly to the preceding illustration, Half of the efficiency achieved for optimal intake energy, or a 39.5% efficacy decrease, might result from a 6-dB decrease in intake control. Biasing results in efficiency loss whenever input power is decreased since the output load is built for constant input energy. Technologies for improved efficiency try to alter output load or biasing to increase effectiveness with less power input.

Doherty Technique

In 1936, W.H. Doherty devised a novel combiner built for radio stations employing high-power tube amplifiers. A λ/4 transmission line may be utilized as a combiner at the output of power amplifiers to generate a linear output power. The traditional DPA comprises two amplifiers: the carrier (primary) amplifier and the auxiliary (peaking) amplifier. A class AB amplifier is utilized for the carrier amplifier, while a class C amplifier is used for the peaking amplifier. The RF input signal is divided between the two amplifiers, where the carrier amplifier is functioning all the time and should nearly achieve saturation at the back-off input power owing to seeing a high impedance, which produces a shift in the load-line. At the same power level, the auxiliary amplifier functions solely in the Doherty area and begins feeding current to the output until it gets saturated at the peak region when the two power amplifiers deliver their maximum specified output power (Abdulkhaleq et al., 2019).

When amplifying RF signals with high peak-to-average power ratios, constant-voltage LPAs are inefficient (PAPR). Thus, improved PA methods are developed to attain great efficiency and linearity. The Doherty, EER, and ET methods are a few of the well-known advanced PA strategies covered in this subsection (Dhar et al., 2020).

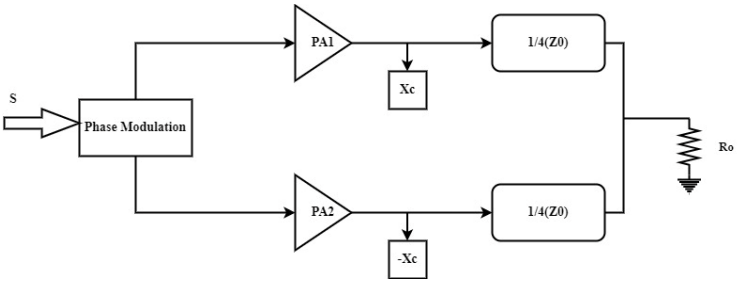

Figure 3. Output phasing amplifier of Doherty is adopted from Singh and Malik, (2021).

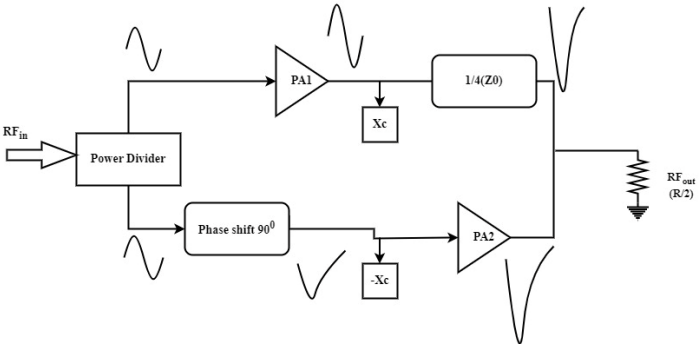

Figure 4. Output phase of the Doherty amplifier Adopted from Singh and Malik (2021).

The power is split between two power amplifiers (PAs) by means of a device known as a power divider circuit. The current drops by half for every 6 dB of PBO. Even when the amount of input power is decreased, the Doherty architecture maintains its high-efficiency level. In order to achieve a PBO of 6 decibels, it is necessary to double the recommended capacity at the outputs from the entire drive casing.

$$R_O\left(6-dBPBO\right)=2R_O\left(fulldrive\right) \quad (8)$$

The main PA stays on permanently regardless of how much electricity is fed into it. In a Doherty design with a 6-dB PBO threshold, the auxiliary PA won't kick on until the input power is greater than the 6-dB PBO threshold.

$$MainPA=\left\{\begin{matrix}P_{FD}-P_{in}\le 6dBON\\P_{FD}-P_{in}>6dBON\end{matrix}\right\} \quad (9)$$

$$AuxiliaryPA=\left\{\begin{matrix}P_{FD}-P_{in}\le 6dBON\\P_{FD}-P_{in}>6dBOFF\end{matrix}\right\} \quad (10)$$

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PFD refers to the maximum amount of input power the PAs are designed to handle. Because of load modulation, the Doherty PA maintains its optimal level of efficiency even when the input power is reduced. Sometimes, with a 6 dB drop in input power from P_{FD}, the effectiveness would not change for the current scenario since it is indicated in the figure below that it will stay the same.

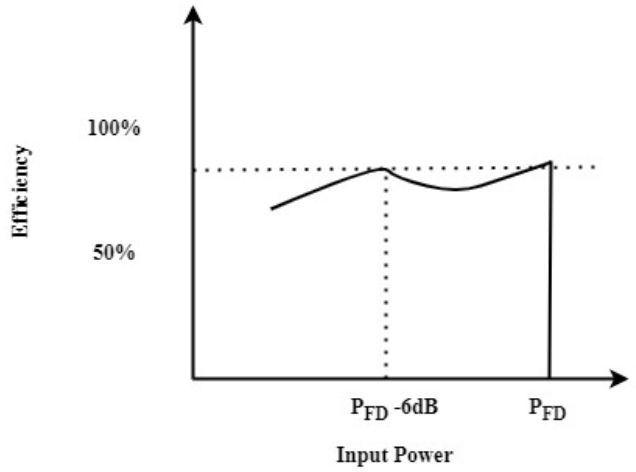

Figure 5. Amplifier Doherty's efficiency is Adopted from Singh and Malik (2021).

One of the biggest issues with a Doherty amplifier's design is regulating the auxiliary PA. It may be used in Class C method, which enables ON/OFF control of the auxiliary PA. Colantonio et al. study (Abdulkhaleq et al., 2019) covered in-depth mathematical study of Doherty PA having primary PA in Class AB type as well as auxiliary PA in Class C type.

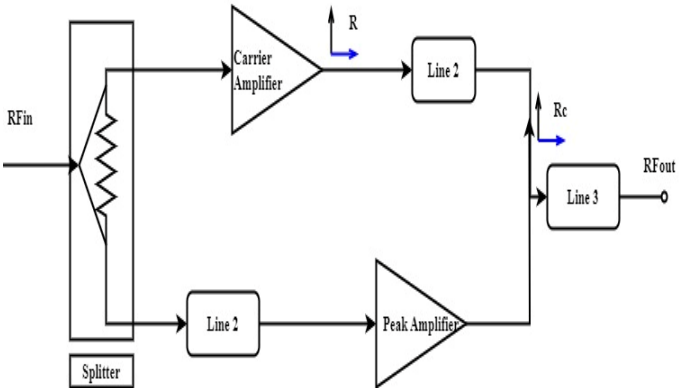

Figure 6. Diagrammatic representation of the even Doherty amplifier is adopted from Sakata et al. (2017).

A class B power amplifier is utilised to show how the Doherty approach works. The dc blocking capacitors are Cblock1 and Cblock2, the RF chokes are Lchoke1 and Lchoke2, the driving signal is V_{gs}, the power amplifier's threshold voltage is V_{th}, the drain current is I_d, the drain voltage is V_{ds}, the power amplifier's dc power supply is V_{DC}, as well as the load resistance, is R (Nikandish et al., 2020).

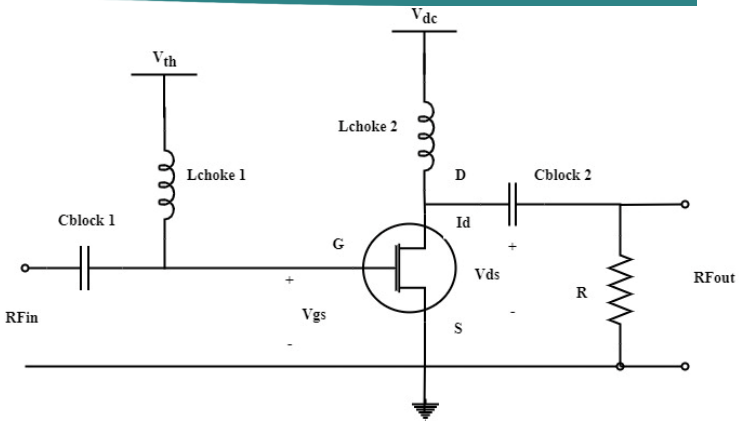

Figure 7. Sakata et al. (2017) adopted a class B power amplifier circuit.

Fig. 8 displays class B power amplifier voltage, current, and load lines. Whenever the highest drain current is Imax as well as this sine wave's fundamental components is a half-rectified sinusoidal waveform, and the operational amplifier is regulated at classes B is I1, as illustrated in Figure 8(a), is

$$I_1 = I_{max} / 2 \quad (11)$$

and the DC component I_0 of I_d can be expressed as

$$I_0 = I_{max} / \pi \quad (12)$$

By multiplying the RF fundamental power output, P1, even by input power from V_{DC}, P_{DC}, the DE may be computed. Thus, according to (11) and (12), the DE can be calculated by

$$DE = \frac{P_1}{P_{DC}} = \frac{V_1.I_1}{V_{DC}.I_0} = \frac{\frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_{max}}{2\sqrt{2}}}{V_{DC} \cdot \frac{I_{max}}{\pi}} = \frac{\pi}{4} \quad (13)$$

From (13), it is clear that the fully powered class B power amplifier, hypothetically, may attain /4 efficiency voltage swing of vds and peak current of id does half reduce each, and the 12 and 13 can be written as

$$I_1 = I_{max} / 4 \quad (14)$$

$$I_0 = \frac{I_{max}}{2\pi} \quad (15)$$

$$DE = \frac{P_1}{P_{DC}} = \frac{V_1.I_1}{V_{DC}.I_0} = \frac{\frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_{max}}{2\sqrt{2}}}{V_{DC} \cdot \frac{I_{max}}{\pi}} = \frac{\pi}{8} \quad (16)$$

While the input RF power is reduced by 6 dB, the class B power amplifier's main waveforms are shown in Fig. 8(b) (a).

When power backing is increased, the DE of the standard class B power amplifier reduces wn, as can be observed by analyzing (13) & (16).

In Figures 8(a) and (b), the class B power amplifier's load resistance is R, but in Figure 6 it is 2R. (c). because the input power is equal as in Figures 8(b) & (c), the peak

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current of id is also equivalent. Nevertheless, the increasing load resistance in Figure 8(c) causes the voltage variation of vds to rise. The DE may now be stated as

$$DE = \frac{P_1}{P_{DC}} = \frac{V_1.I_1}{V_{DC}.I_0} = \frac{\frac{V_{DC}}{\sqrt{2}}.\frac{I_{\max}}{4\sqrt{2}}}{V_{DC}.\frac{I_{\max}}{2\pi}} = \frac{\pi}{4} \quad (15)$$

$$Z_3 = \frac{R_c.(i_{CS1}+i_{CS2})}{i_{CS1}} = R_c.\left[1+\frac{i_{CS2}}{i_{CS1}}\right] \quad (17)$$

A simulation using the quarter-wave transmitting line's characteristics has been done in (Waykole & Bendre, 2018).

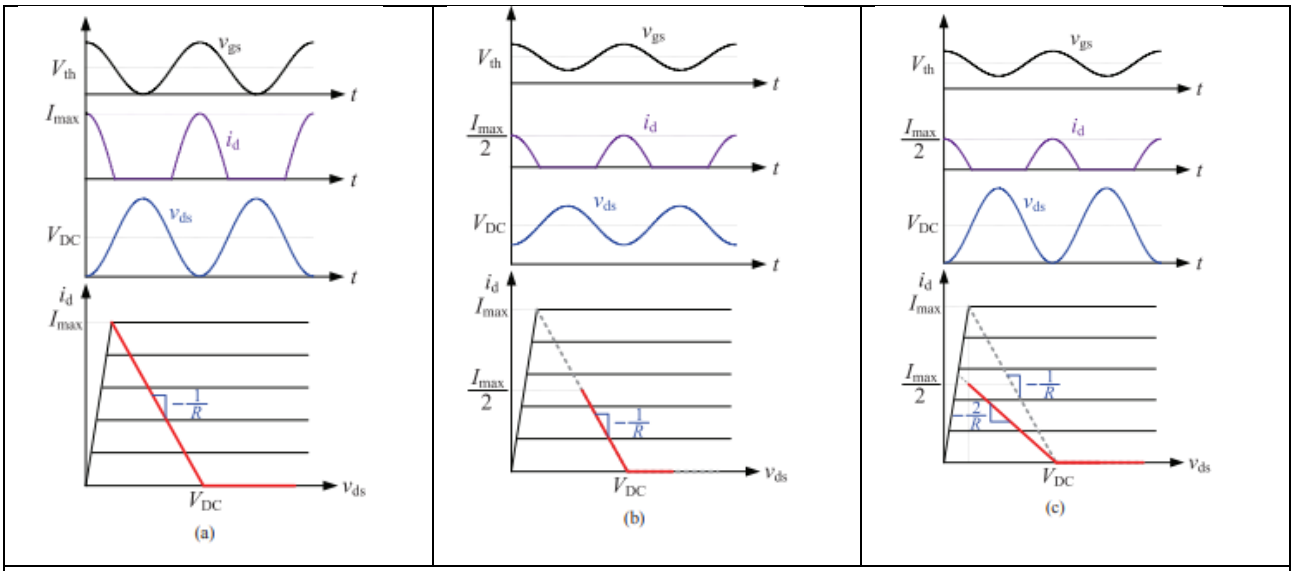

Figure 8. Class B power amplifiers' current waveforms, voltage, as well as load lines. (A) Fully driven with R serving as load resistance. (b) A back-off of 6 dB with load resistance R. (c) 6 dB back-off with resistance from the load is adopted from Sakata et al. (2017).

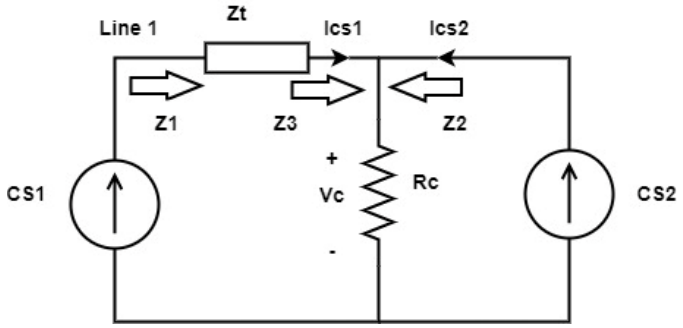

Figure 9. Active load-pull technique is adopted from Sakata et al. (2017).

From (17), raising load resistance can enhance DE when the input RF power is low, as seen in Figure 8(c). This is the Doherty approach. In conclusion, a carrier amplifier with low input RF power needs large load resistance to produce high DE. As RF power increases, load resistance lowers. Active load-pull is used to match load resistance to input RF power (Sajedin et al., 2019).

Figure 9 depicts the modified conceptual construction of the Doherty amplifier to demonstrate the active load-pull technique. Rc serves as their common load, and CS1 and CS2 reflect the carrier amplifier & peak amplifier individually and the ZT impedance of line 1.

According to Figure 9, V_c can be expressed as

$$V_c = R_c.(i_{CSI}+i_{CS2}) \quad (16)$$

Thus, the resistance Z_3 can be expressed as V

$$Z_1 = \frac{Z_T^2}{Z_3} \quad (18)$$

As a result, iCS2 allows for the adjustment of CS1, Z1, and Z1 lowers as iCS2 increases.

Nguyen et al. (2018) demonstrated a 2-stage Doherty PA for 5G employing a stacking field-effect transistor. Dual-driver architecture was employed to boost amplifier output. Around 28 GHz, a power output of 28.7 dBm was recorded as 14.4 dB of gain. The structure is as follows of 37%, with PAE at 6-dB PBO of 27%.

Yamaguchi et al. (2020) demonstrated a 3-stage Doherty amplifier for 28-GHz 5G. Maximum output of around 8 watts & PAE of 24% at 6-dB PBO was attained at the operating frequency of 27 to 29.5 GHz.

A single-stage, asymmetric Doherty PA for 28 GHz was introduced. A Doherty PA with identical primary as well as auxiliary processors, is said to be symmetrical. With PAE—40%, a saturation power output of 22.4 dBm was attained, while at 6-dB PBO, PAE reached a level of 28% (Pae and Abstract, 2018).

Chen et al. (2018) created a transformer-based Doherty PA that uses CMOS technology and operates across 28.7 and 41.9 GHz. Assuming a PAE of 32%, the PA generated 20.7 dBm of power. PAE of 13.1% was reached at 6-dB PBO. Using SiGe BICMOS, a Doherty PA operating at 39, 37 & 28 GHz was created (Hu et al., 2019). Transformers

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were familiar with the Doherty architectural compactness. At 28 GHz with 20.3% PAE and 37 GHz with 22.6% PAE, the PA production was 16.8 dBm and 17.1 dBm, respectively.

Table 2. Overview of CMOS DPAs under review.

Ref	Frequency GHz	Output power P_{linear} dBm	Overall PAE, %	Back-off power Range, dB
(Nguyen et al., 2018)	28	28.7	37%	6
(Yamaguchi et al., 2020)	28	39	30%	6
(Pae & Abstract, 2018)	28	22.4	40%	6
(Chen et al., 2018)	28.7-41.9	20.7	32%	6
(Hu et al., 2019)	28,37,39	16.8,17,17.1	20.3,22.6,21.4%	6.7

EER Technique

Leonard R. Kahn (Kahn, 1952) created the EER technique for the first time in 1952, and it has since attracted a lot of interest. Figure 10 depicts the conceptual layout of the EER approach and the key wavelengths. It demonstrates how the RF input data, which contains both amplitude and phase characteristics, is handled through two pathways: the envelopes path and the phases pathway. The envelopes of the RF original signal, which would be picked up by the electronic filter in the envelope path, determine the supplying modulator's referencing transmitter.

A voltage is delivered by the provided modulating to the nonlinear power amplifiers, which follow the Input signal transmission pulses. Except for the phasing component of the RF input and a signal containing continuous amplitude remains after the limitation eliminates the envelope data from the phases channel. The voltage level given by the supplied modulation restores the amplitude values. The delaying element synchronizes the phase path as well as the envelope path.

Since the EER approach uses an NLPA, high efficiency can be attained. The NLPA functions similar to a high-efficiency LPA thanks to the addition of the supply modulator, which modulates the NLPA's source voltage (Sajedin et al., 2019).

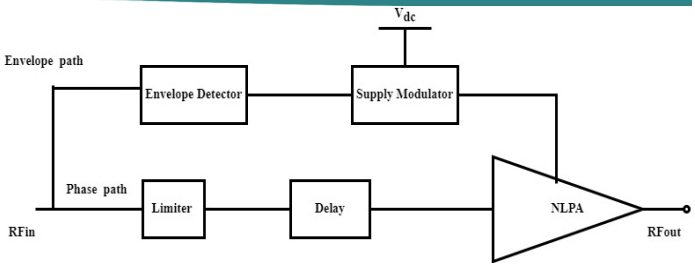

Figure 10. EER method schematic layout and important waveforms [Adopted from Sakata et al. (2017)].

Ref	Process	V_{DD}, V	Frequency GHz	P_{Linear} dBm	PAE,%
(Woo et al., 2014)	320nm CMOS	3.4	2.4	24.3	42
(Woo et al., 2015)	280nm CMOS	3.4	0.837	25.9	42.3
(Park et al., 2016)	180nm CMOS	4.7	1.7	28.5	36.6
(Hassan et al., 2013)	180nm CMOS	3.3	2.535	28.3	48
(Kwak et al., 2012)	150nm CMOS	5	2.5	27.6	46

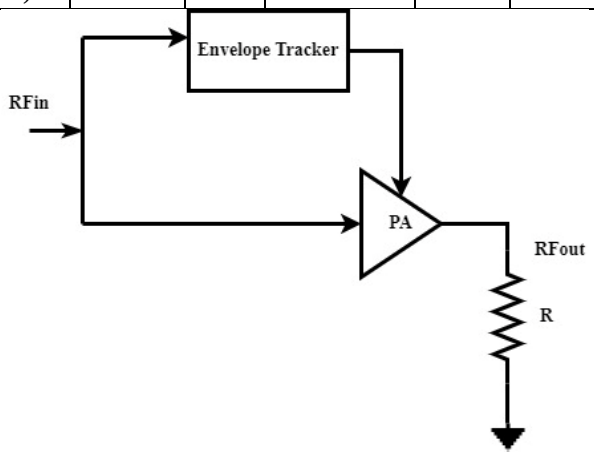

Figure 11. Envelope Tracking [Adopted from Singh and Malik (2021)].

Once the envelope signal has been formed after shaping, a modulator circuit that can provide DC supply in accordance with the envelope signal is needed.

Different modulator circuits exist, including boost mode supply modulators, multimode supply modulators, and hybrid switching amplifiers. The most well-liked one is the hybrid switching amplifier (HSA). HSA combines a switching amplifier with a linear amplifier. While switching amplifiers are used to follow the envelope signal's low-frequency components, linear amplifiers are used to track its high-frequency components.

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According to Kimball et al. (2006), a WCDMA base station PA was created utilizing GaN HFETs. The PA uses ET to provide an average output power of 37.2 W with a gain of 10 dB and an average efficiency of 50.7%.

The envelope tracker was designed with a few key factors in mind. Time mismatch between the input to PA and the envelope signal is among the most significant. The input to PA and the envelope signal must be synchronized at the right time for the best performance. 100 MHz is thought to be the sub-6 GHz 5G bandwidth. For this frequency bandwidth, ET requires a 125 MHz frequency band. It was characterized as a Class-AB PA with a feedback control switching sequence (FFFS) buck - boost converter operating at 88% by Paek et al. (2022).

Matching is another problem with ET amplifier design. Since input voltage may affect output or input capacitances in real devices, designing a corresponding circuit is difficult since a difference in supply voltage would result in a variation in capacitors.

ET may be utilized in conjunction with Doherty and out phasing architecture to increase efficiency. The benefits and encounters of the ET architecture are shown in Table 4.

Table 4. Advantages and Challenges in ET Architecture.

Advantages	Challenges
Can provide extremely high efficacy.	The bandwidths of the envelopes monitor are rather high in comparison to the incoming RF signal.
Due to input DC power being constantly optimised, thermal issue is decreased.	A broad bandwidth should have a minimal temporal offset among the input RF signal as well as the envelope output.

Figure 12 demonstrates the ET approach, which is analogous to the EER technique, as shown in Figure 13, along with its schematic diagram and essential waveforms. The main differences between them can be boiled down to the following: 1) In the EER method, an NLPA is utilised, while the ET technique uses an LPA; in the ET method, the power amplifier amplifies alike amplitude as well as phase information from the RF signal, while the RF signal in the EER method hardly amplifies phase information; in the EER method, the supply modulator's function is to reinstate the amplitude in the initiation of the output RF wave (Barmala, 2019).

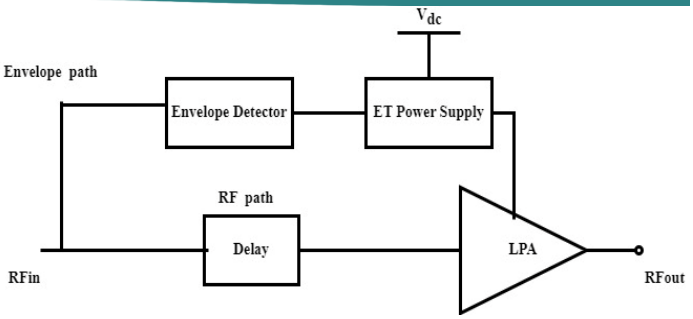

Figure 12. ET technique's flowchart and important waveforms [Adopted from Sakata et al. (2017)].

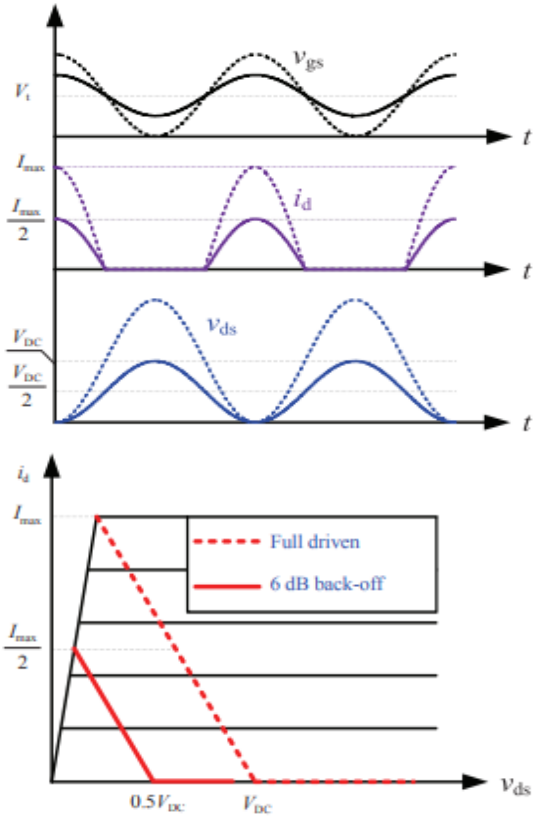

Figure 13. Class B power amplifiers with varied power levels utilize the ET technique, which includes voltage as well as current waveforms with load lines [Adopted from Sakata et al. (2017)].

The class B power amplifier's major waveforms employing the ET approach are shown in Figure 14 at various power levels. The efficacy of the class B power amplifier can approach /4 when it is fully driven, as seen by the dotted lines. With less RF power being supplied, the ET power supply produces less voltage to power the LPA. Solid lines at 6 dB back-off in input power show the class B-powered amplifier's primary wavelengths. The DE is now expressible as

$$DE = \frac{P_1}{P_{DC}} = \frac{V_1.I_1}{V_{DC}.I_0} = \frac{\frac{V_{DC}}{2\sqrt{2}}.\frac{I_{\max}}{4\sqrt{2}}}{\frac{V_{DC}}{2}.\frac{I_{\max}}{2\pi}} = \frac{\pi}{4} \quad (19)$$

From (21), By constantly modifying to use the LPA's voltage levels, the ET approach could also obtain a

significant DE inside the power back-off site (Waykole and Bendre, 2018).

Implementation of ET method and measurement results

Using 0.18-Mm CMOS technology, the supply modulation and PA are produced. The PA is put to the test utilising a 1.85 GHz LTE broadcast with a LO-MHz BW, 16-QAM, and 7.5-dB PAPR. Two manufactured semiconductors have already been linked for evaluation on a two-layer PCB. Employing the designated dynamical circuitry, the ET PA, as well as the standalone PA, as well as the ET PA utilizing constant feedback as well as gate bias are the three scenarios shown in Figure 15 in addition to the parameters of average output power for the ACLRE-uTRA, amplitude, as well as PAE measurements. In comparison to the ET PA without the control, the ET PA with a dynamic controller unit increases PAE by 5% & lowers amplitude variation by 2 dB. Associated with the stand-alone PA, the ET operation lowers the total current consumption for the LTE signal by up to 37%, depending on the power level.

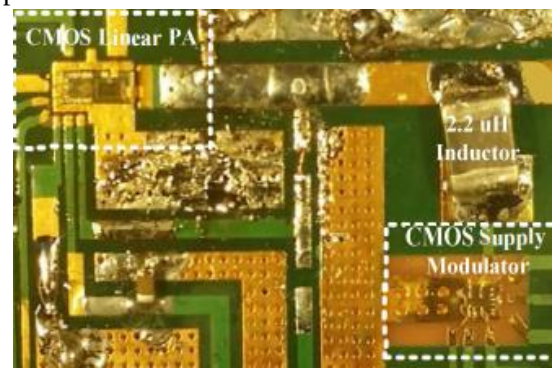

Figure 14. CMOS ET PA module microphotograph showing the linear PA and supply modulator [Adopted from Cabrera and Rangel de Sousa (2020)].

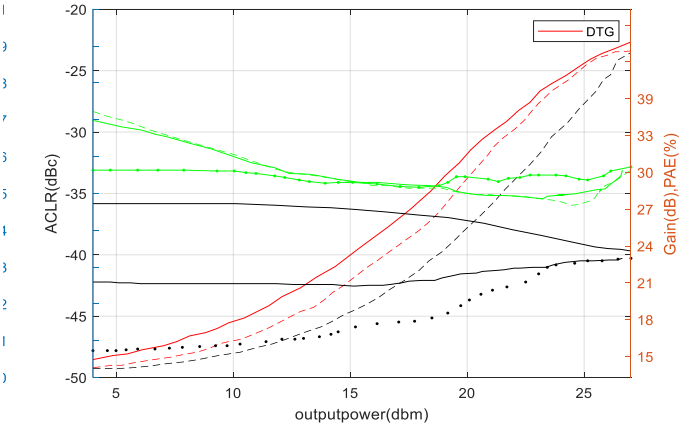

Figure 15. Outcomes of 1.85 GHz tests using the LTE signals for the suggested CMOS ET PA with a dynamic controller unit, traditional ET PA, as well as stand-alone PA without a dynamic controller unit [Adopted from Cabrera and Rangel de Sousa (2020)].

At an averaged power output of 26.5 dBm, the proposed ET PA generates an ACLRE-uTRA level -33.3 dBc as well as a PAE of 35.4%. According to the evolving international radio communication accessibility (E-UTRA) requirements, the ACLRE_ UTRA is evaluated employing a 9 MHz accuracy BW at a central wavelength as well as a 10 MHz offset. Per the LTE spectrum mask, Figure 16 shows the measured spectrum of the solitary PA and ET PA at a median power output of 26.5 dBm (a). The observed far-out emissions spectrum of the ET PA and one PA is shown in Figure 16. (b). Due to the sweet-spot identification used in the ET procedures, the ACLR of the ET PA and the stand-alone PA are both -33.3 dBc, which is 3.3 dB more than the stand-alone PA. As a consequence, the spectra's internal skirt becomes better while its outside skirt kind of gets worse. The ET PA exhibits less spectrum regrowth than the standalone PA up to a 50 MHz deviation from the central wavelength with no discernible peak. The emissions spike caused by the source signal's source signal's sampling rate at the l20-MHz offset may be further reduced by filtration at the transmitters.

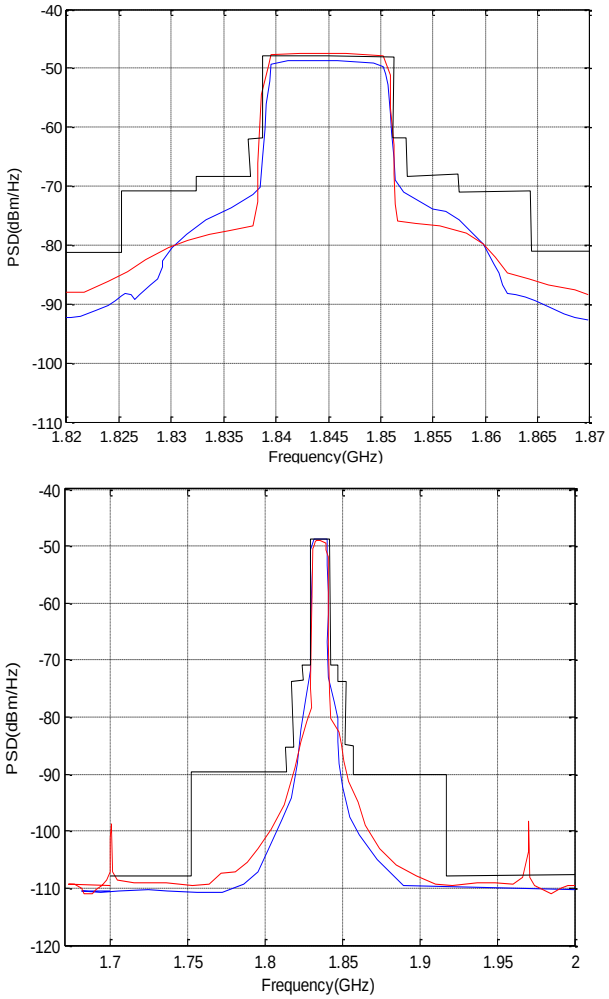

Figure 16. At an averaged output power of 26.5 dBm for both the suggested CMOS ET PA and stand-alone PA, the following spectra were measured: ranges of (a) 50 MHz and (b) 300 MHz. [Adopted from Cabrera and Rangel de Sousa (2020)].

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Comparison of Efficiency Enhancement Techniques

Due to its straightforward structure, mobile communication operators frequently use the Doherty approach in their base stations.

The Doherty method, however, has a number of drawbacks: In order to realise impedance transformation, it requires quarter-wave transmission lines, which limits its use in broadband applications. Furthermore, whenever a NLPA is used to construct the peak amplifier, the peak amplifier's linearity is impaired because output power backing off happens at low output power, leading to poor effectiveness once amplification impulses with extremely high PAPR. In conclusion, the Doherty amplifier cannot satisfy the requirements of upcoming mobile communications technologies, which are primarily appropriate for medium PAPR and narrow-band purposes.

The highest likelihood of achievement lies with the EER approach. Nevertheless, the EER approach also has a few disadvantages: 1) The system's linearity depends entirely on the supply modulator's linearity because it restores the amplitude information; this presents major design issues for the supply modulation scheme; 2) The device's linear relationship is extremely sensitive to the interruption aligning among the packet route and the step trail; any discrepancy would then cause deformation of the RF output signal; as well as 3) The low-frequency band of the EER system would indeed possess a low amplification. Several problems restrict its applicability.

Table 5. Summary of Compared ETs in CMOS PA.

Ref	Process	V_{DD}, V	Frequency GHz	P_{Linear} dBm	PAE,%
(Su et al., 2019)	180nm	1.8-3.3	Sub-1GHz	21.08	37.9%
(Cabrera & Rangel de Sousa, 2020)	180nm	1.8	Sub-1 GHz	14.2	48.1%
(Ko et al., 2018)	180nm	1.8	Sub-1 GHz with 2 modes of operation	12.73	25.6%
(Ko and Nam, 2019)	180nm	3.0	04-1.2 GHz	20.22	36.9%

In contrast to the EER technique, the LPA primarily determines the linearity of the ET systems. Hence, the uniformity criteria of the ET power supply are less stringent, providing for a wider range of output voltage options. The frequency demands for the ET power source might be decreased as a consequence. Meanwhile, the precision of the delayed mismatch between the envelope route and RF path in the ET approach may be diminished, which may affect the RF output signals. Due to these benefits, the ET method is more suited for broadband applications. Additionally, the envelope shaping used in the ET approach results in a larger gain in the low output power area, preventing gain collapse and enhancing system linearity (Yu et al., 2020). Because of this, the term "width quantization" refers to the method used to specify a FinFET device's channel width in terms of FIN height. The charging movement in the FinFET might be enhanced by increasing the fins in the architecture, giving the gates greater control over the channel charges. The structure's fin count may be increased in order to achieve this. A quantifiable parameter used to characterize the structure's stability is the fins' height. For example, a structure with a short fin height will be more flexible than one with a long fin height (Ensan et al., 2019).

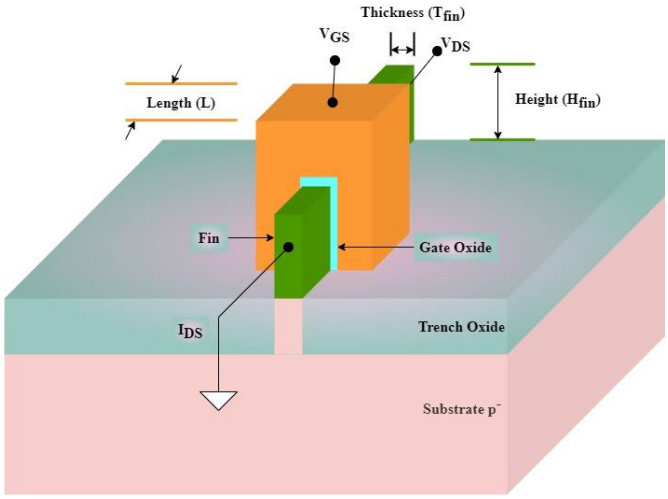

Figure 17. SOI FinFET.

It is also possible to implement FinFETs on bulk wafers, in which case all of the fins will share the substrate. The migration from bulk MOSFETs to bulk finFETs is a straightforward process. In planar SOI FinFETs, the fins are separated from one another. Figure 18 presents an analysis of the differences and similarities between SOI FinFET and bulk.

Characteristics of FinFET

Right now, we're discussing FinFET's electrostatic characteristic (Current-voltage). The defining characteristic of a FinFET is the formation of the gate,

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which consists of a conductive channel surrounded by thin "fin" silicon. The fin's thickness from the source to the drain is determined by the direction that establishes the device's effective channel width. In order to create numerous gate electrodes on either side of the channel and reduce leakage currents while increasing drive current, The channel is encircled by the gate electrode. The vertical si fin is controlled by a self-aligned double gate for the FinFET (Atalla et al., 2020).

For a given Vg > Vth, the linear region is the area where Ids increase linearly with Vds. Ids is given in the linear sector as the first approximation of

$$Ids = \frac{\mu W}{L} KT \frac{Vg - \Delta\phi}{KT}\left(1 - e^{q}\frac{(Vds)}{KT}\right) \qquad (20)$$

Carrier mobility in the inversion zone, also known as the channel, is Cox, which is indeed the oxide thickness capacitor per unit of area, W/L is the device's breadth to length equal, and Vth is the threshold voltage.

Saturation Region: While Vds are rising in this region, Ids are becoming steady. Once more, the Ids are in the saturation region specified by the initial preliminary computation.

$$Ids = \frac{\mu CoxW}{L}\left\{\frac{V_g - V_t}{2m}\right\} 2, m = 1 + 3(tox / xd) \qquad (21)$$

The depletion layer's thickness, xd, and the oxide's thickness, t_{ox}, demonstrate that Ids are independent of V_{ds}.

Cut-Off Region: In this region, V_g is smaller than V_{th}, preventing a channel from forming between the source and drain, causing I_{ds} to equal 0. The exponential decay current flows as the sub-threshold current for V_g V_{th}.

Sub-threshold current is mainly caused by carrier diffusion as a result of a strong electrical field along the channel caused by low electron concentration. This area's current is roughly represented by

$$Ids = \frac{\mu W}{L} KT \frac{Vg - \Delta\phi}{KT}\left(1 - e^{q}\frac{(Vds)}{KT}\right) \qquad (22)$$

$\Delta\phi$ is the distinction among the gate electrode's purpose and the nearly invasive silicon skin (Chandra and Kishore, 2019).

Predictive Technology Models for FinFET

Before a future technology is completely constructed, it is always necessary to research its aspects using an accurate and modifiable model. In analyzing the creation of future circuits, using Predictive Technology Model (PTM) files for future transistor and interconnect technologies is an extremely important step. The PTM files are compatible with conventional circuit simulators and are expandable to accommodate any process changes (Mukku et al., 2020). The Berkeley Predictive Technology Model (BPTM) transitioned into the PTM, which includes innovative elements such as predicting new methodologies and scalable devices for FinFET. A significant amount of investigation has been carried out in order to gain an understanding of the underlying physics of the FinFET device (Tripathi et al., 2021).

After reviewing the relevant research (Jain and Tomar, 2020), it has been established that the thermal effect, mobility, and Vth are likely to remain unchanged during the scaling process. The research was able to evaluate the performance of the suggested CMOS circuits with the performance of standard CMOS circuits with the assistance of predictive modeling of CMOS devices that are relevant toward the 32nm node (Pandey and Pandey, 2020).

Comparison of FinFET with CMOS Device

The physical and electrical properties of the CMOS device are used to compare the FinFET device's features and characteristics to those of the CMOS device (Vashishtha and Clark, 2021).

Drawbacks in CMOS device

- The scaling of the MOSFET transistor, which has led to improvements in transistor densities and efficiency, has a drawback known as the leaking issue. Reducing oxide thicknesses, increasing substrate doping, and shortening of channel lengths all contribute to an increase in leakage.
- The leakage problem is made significantly worse by lowering the threshold voltage, which is done to improve performance at lower working voltages.
- The DIBL issue is made worse by the reduction in the size of the drain and resources, which adversely affects the gate's ability to manage the channel effectively.
- In the not-too-distant future, according to projections, the dynamic power consumption of static power dissipation should surpass each device (Chaves De Albuquerque et al., 2019).

Efficiency of FinFET technology

- Current will move from the drain to the source when a voltage that is theoretically greater than the threshold voltage is put across the DG device's gates. Contrarily, the twin gates enable the channel to be modulated from two sides as opposed to simply one. When combined, the channel potential is significantly affected by the two gates, which helps mitigate the effect of the drain and ultimately results in an enhanced capacity to cut off the channel current.
- The DG device allows for a reduction in DIBL, which results in an improvement in swing.

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- Recent research efforts have centered on FinFETs, even though various variants of double gate transistors have been examined.
- There is a good chance that FinFETs will be a contender due to the relatively low production costs, its twin gate's organically existing arrangement, and its capacity to route (Mohammed et al., 2021).

Complexity in FinFET device design

- It is important that the fin height, denoted by Hfin, be the same for each and every fin on the chip. Processing becomes more difficult and errors become more likely with increased height.
- To optimise on current (Ion) while reducing leakage current (Ioff), and to maximise the on current, I_{on}. To combine elevation, fin thicknesses, oxide thickness, as well as channel width. This causes the process of fin engineering to become more complicated.
- The size of FinFETs is difficult because broader devices are made using numerous fins.
- Determining the ideal number of parallel fins for every circuit gate is what the FinFET sizing process comes down to at the end (Mohammed et al., 2021).

V-I Characteristics of FinFET

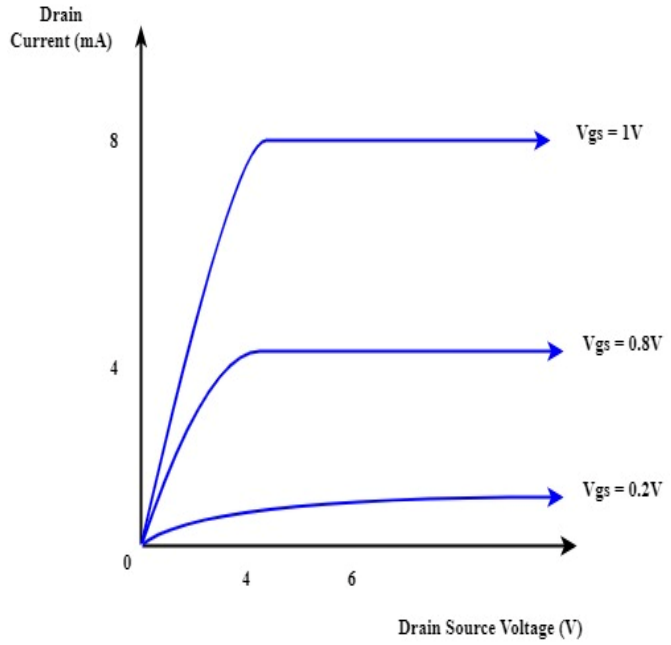

Figure 18. V-I characteristic of FinFET.

The application of the drain-source voltage results in an upsurge in the drain current. At first, there is a linear rise, and then, after that, there is an entry into the saturation region, which is the region where the curve is practically at its maximum.

Discussion on the future perspective of RF amplifiers

As a result of the necessity of an amplified radio frequency signal for the effective operation of consumer electronics products, there has been an exceptionally high rate of adoption of RF Power Amplifiers in this sector. Additionally, RF Power Amplifiers are one of the most expensive components of all base stations for wireless cellular and mobile infrastructures. Furthermore, the demand for RF Power Amplifiers is growing as a result of the significant improvements in telecom infrastructure (Razavieh et al., 2019).

Challenges

- A rise in consumer electronics consumption can be seen worldwide, most noticeably in the form of smartphones and tablets.
- It is anticipated that the market for consumer electronics, particularly mobile devices such as smartphones and tablets, will experience significant expansion during the course of the period under consideration.
- Consumer Electronics, a significant application industry for RF Power Amplifiers, will henceforth boost the global market for RF Power Amplifiers. This is due to the fact that consumer electronics is a growing industry.
- In addition, the growing adoption of 4G technology and the introduction of next-generation wireless networks, such as 5G, would be further factors that drive the need for RF power amplifiers and the expansion of the market for these products.
- The high costs of RF Power Amplifiers operate as a significant limitation for the worldwide RF Power Amplifier market, which limits the usage of these devices.
- In addition to this, other challenges, such as RF Power Amplifiers' huge size and high power consumption, are a barrier to their continued development (Callender et al., 2018).

Future Perspective of RF Amplifiers

The market for RF power amplifiers is primarily driven by increased cellular network demand and the implementation of IoT technology. The dynamic nature of the semiconductor sector and high operational costs could limit market expansion. Due to ongoing advancements in RF power amplifiers' linearization and power efficiency, businesses might look for opportunities.

The market for RF power amplifiers is anticipated to expand at a CAGR of 13.37% from 2017 to 2023. Asia-Pacific dominated the market in 2016 with a 41.13% share, followed by North America and Europe with respective market shares of 30.88% and 22.15%. The market expansion in Asia-Pacific is being driven by the rising demand from cellular networks and the rising usage of IoT services across numerous business verticals (Zhang et al., 2021; Varshney et al., 2024).

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The frequency, raw materials, packaging type, application, and region-based segments of the worldwide RF power amplifier market have all been defined. The market is divided into four categories based on frequency: 10 GHz and below, 10 GHz and between, and 30 GHz and beyond. The market is divided into silicon, gallium arsenide, gallium nitride, silicon germanium, and others based on the raw materials used. The market is divided into surface mount, die, standalone/rack mount, and others according to the kind of packaging. The market is divided into consumer electronics, aerospace & defense, automotive, medical, and others on the basis of application. The market is divided into four categories based on region: Europe, North America, Asia-Pacific and the rest of the world.

Conclusion

Over bulk CMOS, FinFET technology has various advantages, including scalability of the transistor beyond 28 nanometers, better mobility, less leakage, and higher driving current for a given transistor footprint. Lower power usage and the absence of random dopant variation outweigh these benefits. FinFETs have replaced planar MOSFETs in the nanoscale space due to the latter's difficult implementation. FinFETs prevent short-channel effects more effectively than planar MOSFETs, allowing for the scalability of the transistor. Beyond gate lengths of 30 nm, the planar architecture does not scale well. The source's gate control is no longer sealed within by the gate oxide, and the drain is now weak. The control only extends to the area immediately below the gate, even with a perfect gate dielectric of thickness zero. The leakage current, however, cannot be controlled because it is too distant from the gate interface. It becomes more challenging to turn off the transistor as the off-current increases and the subthreshold slope deteriorates.

Electrostatic control can be improved by removing the leakage current. Making use of a multiple-gate structure is one method. Because the leakage current is always in the channel's middle, the current is decreased by making the channel thinner. The gate-all-around transistor is anticipated to replace the FinFET in the future.

The need for high data transmission rates has driven the continuous development of mobile communication systems. As a consequence, spectrum-efficient modulation schemes were used, which may be identified by their high PAPR and fluctuating RF signal envelope. The LPAs are used to fulfil the RF output signal's stringent linearity requirement. However, constant voltage-powered LPAs have a low efficiency. In the aim to suggestively upsurge the effectiveness of the power speakers, the Doherty, EER, and ET techniques—three widely used effectiveness-enhancing methodologies have been investigated in this study. The ET approach is found to be most suitable for developing wireless telecommunications networks after the working principles and characteristics of every technique are analysed. The essential element, the ET power source, has a considerable impact on the effectiveness of the ET systems.

Conflict of Interest

The authors declare no conflict of interest.

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